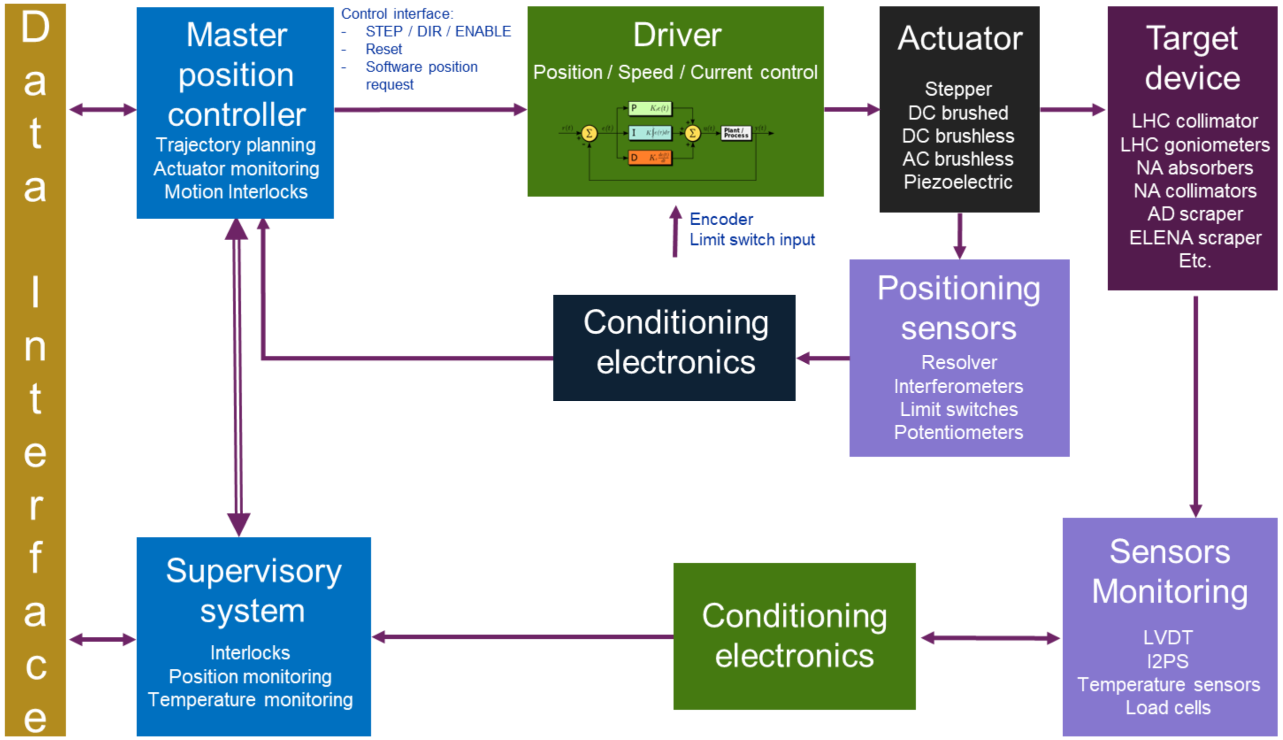
Future procurements at CERN in Instrumentation & Control and CODAC

Alessandro Masi, CERN

Sensors Acquisition & Motion Control (SAMbuCa)

- Flexible and modular low-level control solution for mechatronics devices to provide a standard mechatronics control solution (i.e. standard HW building blocks & API) for the Accelerator Technology Sector

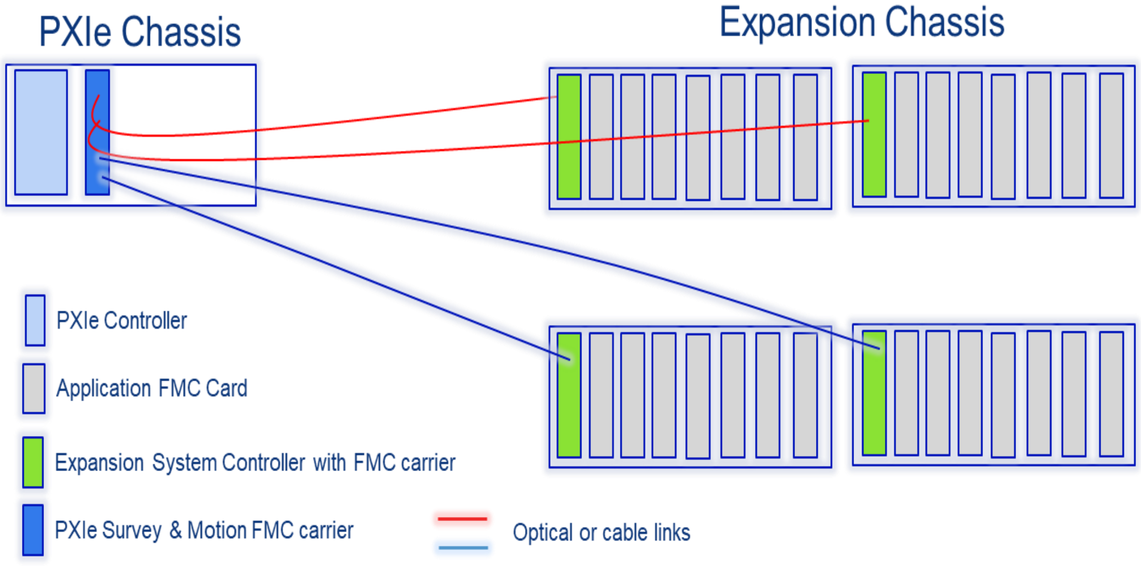
- Low level:
  - ✓ Hard RT constraints → FPGA-based controllers
    - ❑ timing synchronization (i.e. White Rabbit)
    - ❑ µs response time
- User friendly API to profit of all the hardware features



SAMbuCa architecture

Sensors Acquisition & Motion Control (SAMbuCa)

We are looking for industrial partners !

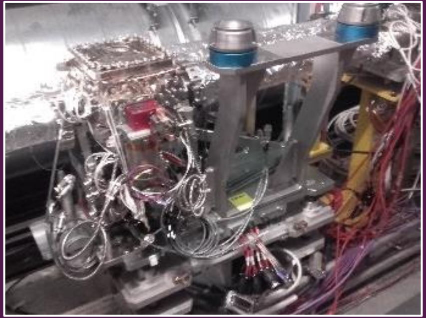


- ✓ **PXIe front-ends**
- ✓ **PXIe carrier card**:
  - ✓ equipped with a large FPGA for data processing and RT control
  - ✓ can host one FPGA Mezzanine Cards (FMC) to ensure the interface with the field instrumentation, sensors and actuators
- ✓ **Set of FPGA Mezzanine Cards (FMC)** to cope with the various field control and instrumentation applications (LVDT, resolvers, IOs, strain gauges, interferometer reading, motor drivers)
- ✓ **Expansion chassis** ensures modularity. It is equipped with a system controller linked and synchronized to the PXIe carriers via White Rabbit

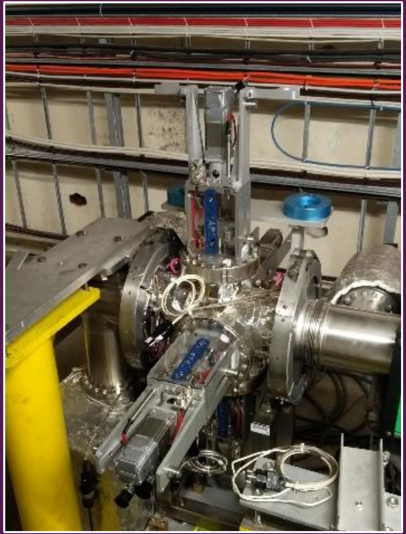
SAMbuCa: CERN Scope

LHC Collimator

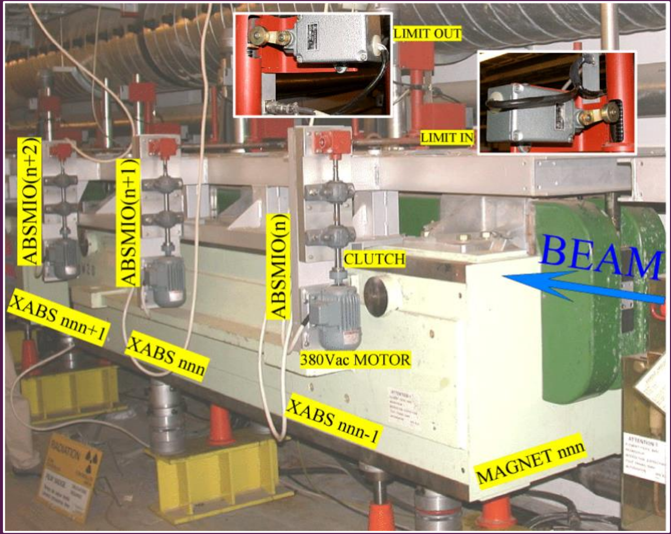
LHC crystal goniometer



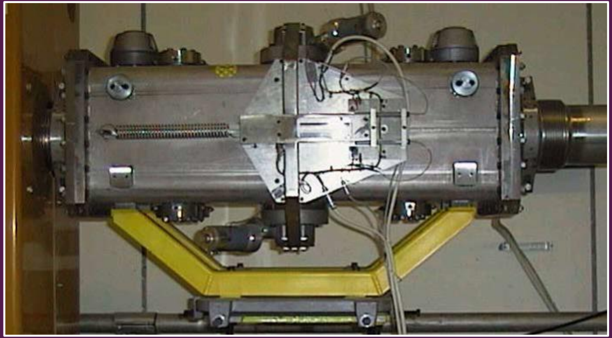
ELENA & AD scrapers



NA absorbers



NA collimators



Actuator

Stepper
AC brushless
Piezoelectric

Target device

LHC collimator
LHC goniometers
NA absorbers
NA collimators
AD scraper
ELENA scraper
Etc.

Positioning sensors

Resolver
Interferometers
Limit switches
Potentiometers

Monitoring sensors

LVDT
I2PS
Temperature sensors
Load cells

SAMbuCa: Actuators compatibility

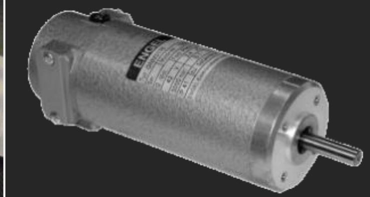
Rad Hard Motors / Actuators up to 30 MGy

Stepper

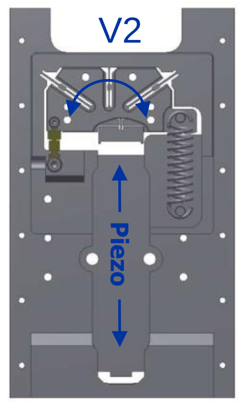
DC brushless

AC brushless

DC brushed



Piezo actuator



Flexural-hinge based rotational stage
Piezo linear movement
No backlash, hysteresis and creep
→ closed loop control

Developed Piezoactuators UHV, HT and Rad Hard

Actuator
Stepper
DC brushed
DC brushless
AC brushless
Piezoelectric

Target device
LHC collimator
LHC goniometers
NA absorbers
NA collimators
AD scraper
ELENA scraper
Etc.

Positioning sensors
Resolver
Interferometers
Limit switches
Potentiometers

Monitoring sensors
LVDT
I2PS
Temperature sensors
Load cells

SAMbuCa: Power Driver

https://indico.cern.ch/event/1115112/contributions/4688938/attachments/2376100/4058940/2022-01-20%20Motor%20Driver%20Overview%20SAMbuCa.pdf

Main features

- ➢ Robust and accurate control of stepper and DC brushed motors in constant current or speed control (including also AC and DC Brushless)
- ➢ Use over long distances with cable length compensation up to 1km
- ➢ standard stepping (open loop) or FOC (closed loop) control via the same interface and hot swappable
- ➢ Kalman Filter for position and torque estimation

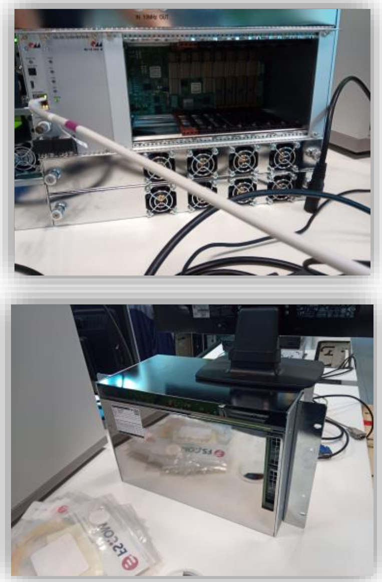
Main specifications

- ✓ Control of 1 stepper motor or 2 DC brushed motors or 1 DC brushless
- ✓ Maximum current per phase: 10 A (rms)
- ✓ Maximum DC voltage: 170 V
- ✓ Communication interface: MODBUS over RS485, PROFINET,
  Standard stepper interface (STEP, DIRECTION, ENABLE)
- ✓ Supports up to 2 encoders
- ✓ Current loop bandwidth up to 1 KHz

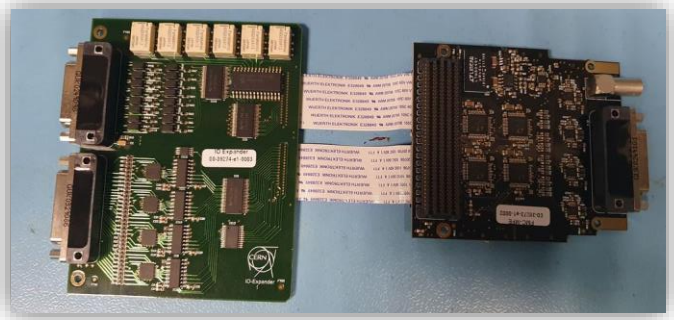
Previous driver version in operation

SAMbuCa: other building blocks

For detailed information: [Home · Wiki · Projects / SAMbuCa · Open Hardware Repository (ohwr.org)]



PXIe standard High Availability Chassis



- FMC cards for step motion control: gateware grbl interpreter based
  - General purpose DI/DO/AI/AO
  - Resolvers, LVDTs, potentiometer front end module

  https://ohwr.org/project/fmc-mfe/wikis

- COM Express CPU

- PXIe carrier card for FPGA Mezzanine Card (FMC) standard

  https://ohwr.org/project/spexi7u/wikis/home

- COM Express-PXIe adapter

  https://ohwr.org/project/pxie-ctl-comexpress/wikis

SAMbuCa: procurement numbers

Item	Tot. Number
PXIe Carrier	**400**
AF Motion Control FMC Card	**400**
COMe – PXIe	**400**
COMe CPU	**400**
Stepping Motor Driver	**1200**

Item	Estimated Budget Range	Market survey by
Stepping Motor Drivers	200k<c<750k	Q2 2024
FMC cards for Motion Control	50k<c<200k	Q1 2024
PXIe-COMe adapter	200k<c<750k	Q1 2024
COMe CPU	200k<c<750k	Q4 2023
PXIe Carrier	200k<c<750k	Q1 2024

Technical responsible: Javier Serrano
Javier.Serrano@cern.ch

Robotics related possible future procurements

- ROV with robotic arm
  - ✓ Minimum 6DoF
  - ✓ ~ 100 kg payload
  - ✓ Minimum speed 2km/h
  - ✓ Battery autonomy > 4hours
- ROV base only
  - ✓ Minimum speed 2km/h
  - ✓ Battery autonomy > 4hours

www.telerob.com

www.hawe.com/it-it/

- Versatile legged and wheeled solutions to reach complicated zoned with robotic arm
  - ✓ ~ 5 kg payload
  - ✓ Minimum speed 2km/h
  - ✓ Battery autonomy > 2 hours

www.bostondynamics.com

www.anybotics.com

- Motion capture system
  - ✓ Area to cover ~ 5 x 5 meters
  - ✓ Sub mm precision
  - ✓ Up to 20 objects to track
  - ✓ > 200 Hz of acquisition rate

https://optitrack.com/systems/

Robotics related possible future procurements

Item	Estimated Budget Range	Market survey by
ROV with robotic arm	200k<c<750k	Q3 2023
ROV base only	<200k	Q1 2023
Versatile legged and wheeled solutions	200k<c<750k	Q2 2023
Motion capture system	<200k	Q1 2023

Technical responsible: Mario Di Castro
mario.di.castro@cern.ch

OASIS overview and future needs

- A distributed oscilloscope application for operators and equipment experts
- 1500 signals acquired by 350 multiplexed digitisers. Using 370 trigger events
- Another 2200 signals from FGCs and 850 signals from other data sources
- Current systems based on Compact PCI and PCI
- Complete consolidation required by LS3 (2028) because of EoL of the installed digitizers

OASIS: high-speed digitizers Technical Specs

For the 2 and 4 GSPS

Characteristic	Minimum requirement
Analogue front-end	
Number of input channels	1
Input frequency range (-3 dB bandwidth)	DC to 3 GHz
Input coupling and impedance	DC 50 Ω
Full scale range (FSR)	1 V
Vertical offset adjustment	± FSR/2
Vertical offset adjustment resolution	FSR / 2^8
SNR (at 1 GHz)	52 dB
SFDR (at 1 GHz)	57 dBc
ENOB (at 1 GHz)	8
Digital conversion	
Resolution	14 bits
Sampling rate (internal clock)	8 GSPS
Samples memory	2G samples per channel
Acquisition modes	Single trigger and multi-record
Record size	Full memory, in one single record or divided for multiple records
Triggering	
Trigger sources	External, internal (channel), software
Trigger slope	Positive and negative
Trigger timestamp resolution	50 ps
Trigger timestamp precision	50 ps
Trigger delay	From 100% pre-trigger (all samples before the trigger) up to 100% post-trigger (all samples after the trigger) independent of record size and acquisition mode
Trigger delay adjustment resolution	1 ns
External trigger coupling and impedance	DC 50 Ω
External trigger level range	0 to 3.3 V

For 1 GSPS specs refer to [Home · Wiki · Projects / FMC ADC 1G 8b 2cha · Open Hardware Repository (ohwr.org)]

1.1.1 Conditions on Linux Device Drivers

1. If the Software includes a Linux device driver, the sources for the driver shall be made available, allowing a full build process. Building of driver binaries and their installation shall be possible through the usual sequence of commands:

```
make -C $(KERNELSRC) M=$(PWD) modules/modules_install
insmod <module>.ko
```

2. *[Incentive option 1]* Sources of kernel code shall be made available under a GPL2 or later license. If not licensed this way, the bid will be taxed with a malus as described in the Tender Form.

1.1.2 Conditions on User Space Libraries

1. If the Software includes user-space libraries, installation of their binaries should reduce to copying the binaries to configurable places, so that relocatable installation is possible, without any intervening hard-coded path.
2. *[Incentive option 2]* Sources of libraries, if made available, shall be licensed under any one of the OSI- and FSF-approved Open Source licenses. If not licensed this way, the bid will be penalized with the malus specified in the Tender Form.

OASIS: high-speed digitizers future tenders

Bits	Sampling Rate	Installed Channel Count	Existing Form(s)	New Form	Estimated Budget	Market survey by
8	1 GSPS	500	50% cPCI, 50% PCI	PXIe (4+ channels per slot)	>750kCHF, <5 MCHF	Q1 2025
10	2 GSPS	45	cPCI	PXIe (2+ channels per slot)	200k<c<750k	End of 2023
10	4 GSPS	20	cPCI	PXIe/PCIe (2+ channels per slot)	<200K	End of 2023
10	8 GSPS	10	cPCI	PCIe (1+ channels per slot)	<200K	End of 2022 (Price enquiry published- Deadline End of Sep 2022)

Technical responsible: Dimitris Lampridis
dimitrios.lampridis@cern.ch

DI/OT project overview and future tenders

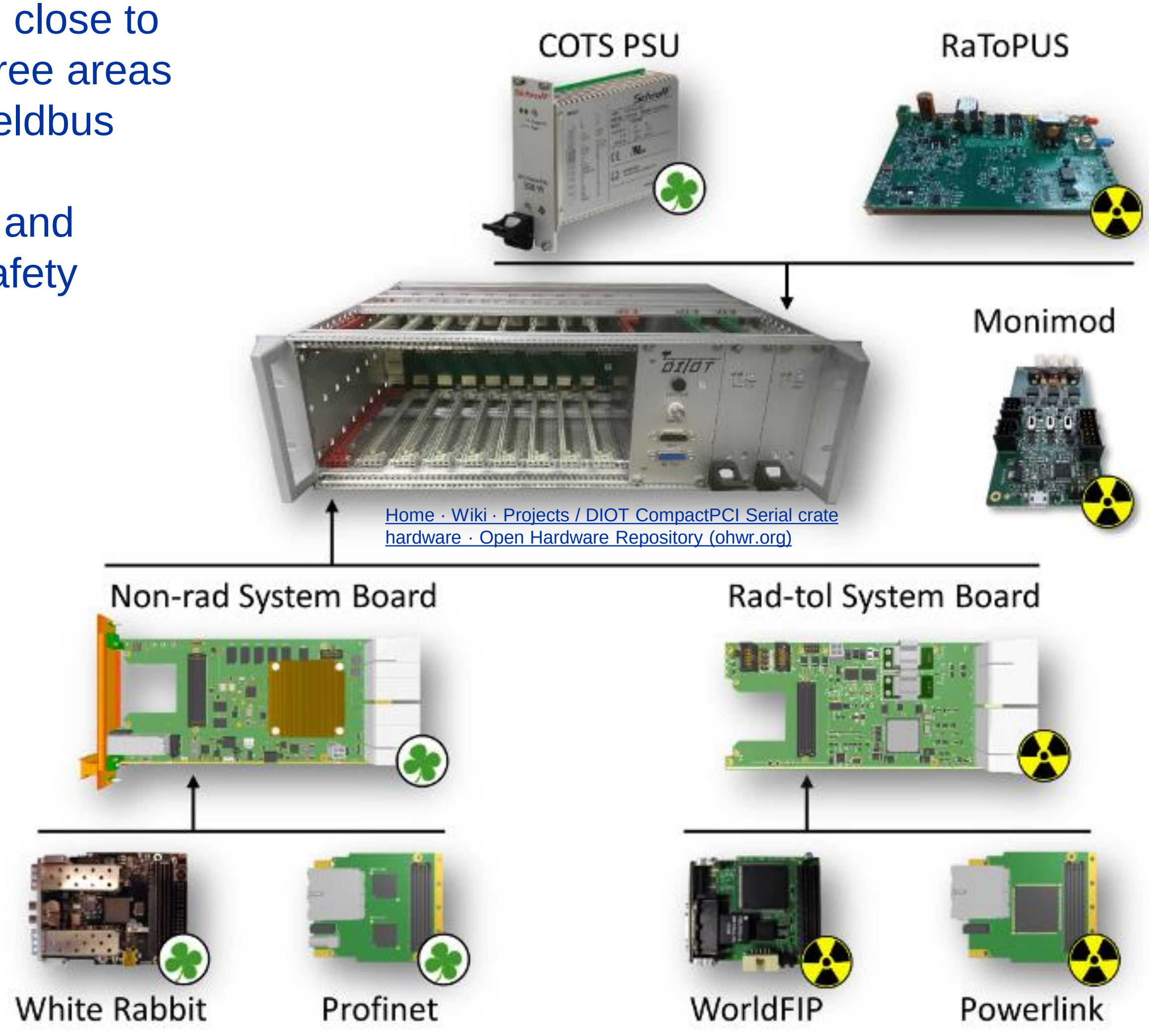
[Home · Wiki · Projects / DIOT - Distributed IO Tier · Open Hardware Repository (ohwr.org)]

- Distributed I/O Tier: where electronics modules installed close to a particle accelerator in radiation-exposed or radiation-free areas controlled by the master in the Front-end tier over the fieldbus

- These are usually FPGA-based boards sampling digital and analog inputs, driving outputs and performing various safety critical operations.

Quantity	Item	Estimated Budget Range	Market survey by
200	DI/OT crate	200k<c<750k	Q2 2023

Technical responsible: Greg Daniluk
grzegorz.daniluk@cern.ch

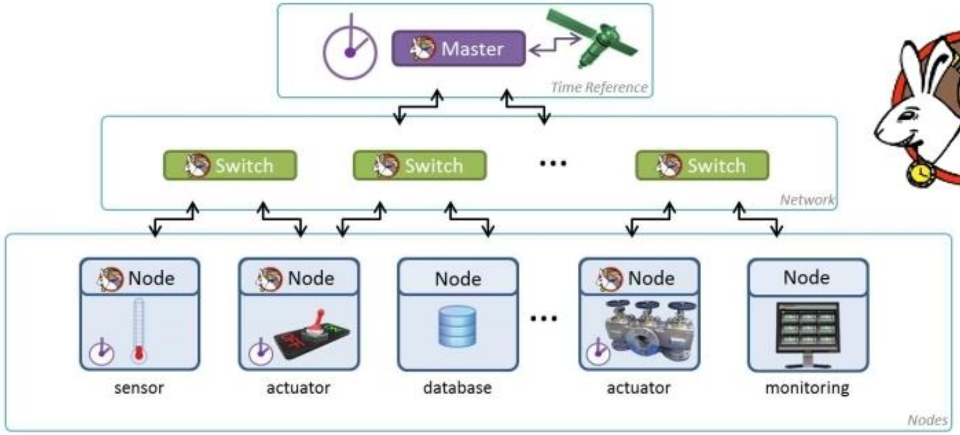


Home · Wiki · Projects / DIOT CompactPCI Serial crate hardware · Open Hardware Repository (ohwr.org)

White Rabbit

Home · Wiki · Projects / White Rabbit · Open Hardware Repository (ohwr.org)

- White Rabbit provides sub-nanosecond accuracy and picoseconds precision of synchronization for large distributed systems (IEEE1588-2008)
- It allows precision time-tag measured data using the same network to transmit data
- It is foreseen to consolidate by 2028 all the CERN accelerator timing (i.e. Rs485 copper based) with WR



Quantity	Item	Estimated Budget Range	Market survey by
150	WR switches v.3 https://ohwr.org/project/white-rabbit/wikis/Switch	200k<c<750k	Q1 2023
100	WR switches v.4 https://ohwr.org/project/wr-switch-hw-v4/wikis/home	200k<c<750k	Q1 2024

Technical responsible: Evangelia Gousiou
Evangelia.Gousiou@cern.ch

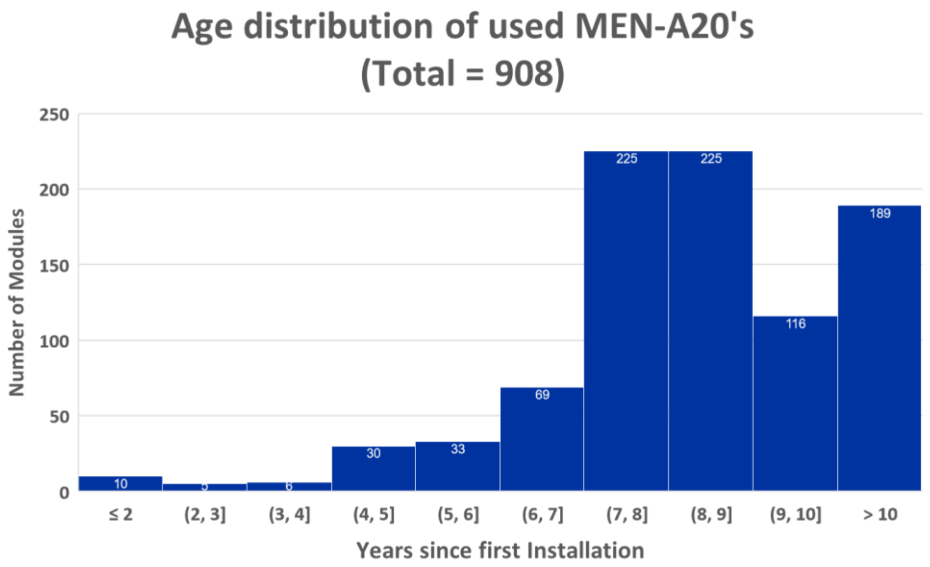
VME System Boards CPU

- More than 1000 VME crates are currently in operation in the CERN accelerator complex as front-ends for controls and acquisition

- Around 900 VME crates are equipped by a system board that will be obsolete by 2028:
  - ✓ Increase MTTF
  - ✓ Memory not enough for new applications
  - ✓ Intel Core 2 Duo not supported by new Linux distribution

- A smooth consolidation campaign will be launched in the next couple of years

Quantity	Item	Estimated Budget Range	Market survey by
1200	VME System Board	>750kCHF, <5 MCHF	Q1 2023



Technical responsible: Erik Van Der Bij
Erik.van.der.Bij@cern.ch

Control and CODAC: CERN tenders overview

	Volume (MEUR)	Major tenders (#)
2022	<200K	*8 GSPS PCIe digitizers*
2023	<200K	*4 GSPS PXIe/PCIe digitizers*
	200k<c<750k	*2 GSPS PXIe digitizers*
	200k<c<750k	*DI/OT Crates*
	200k<c<750k	*White Rabbit Switches v.3*
	>750kCHF, <5 MCHF	*VME System Boards*
	<200K	*ROV base only*
	<200K	*Motion capture system*
	200k<c<750k	*Versatile legged and wheeled solutions*
	200k<c<750k	*ROV with robotic arm*
2024	50k<c<200k	*FMC cards for Motion Control*
	200k<c<750k	*PXIe-COMe adapter*
	200k<c<750k	*COMe CPU*
	200k<c<750k	*PXIe Carrier*
	200k<c<750k	*White Rabbit Switches v.4*
2025		
	200k<c<750k	*1 GSPS PXIe digitizers*

Big Science Business Forum 2022 | CDTI (bsbf2020.org)