Big Science Business Forum 2022

esa

Data Handling, Control systems and Microelectronics building blocks for Space

opportunities to work for ESA projects and technology programs

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Personal self introduction

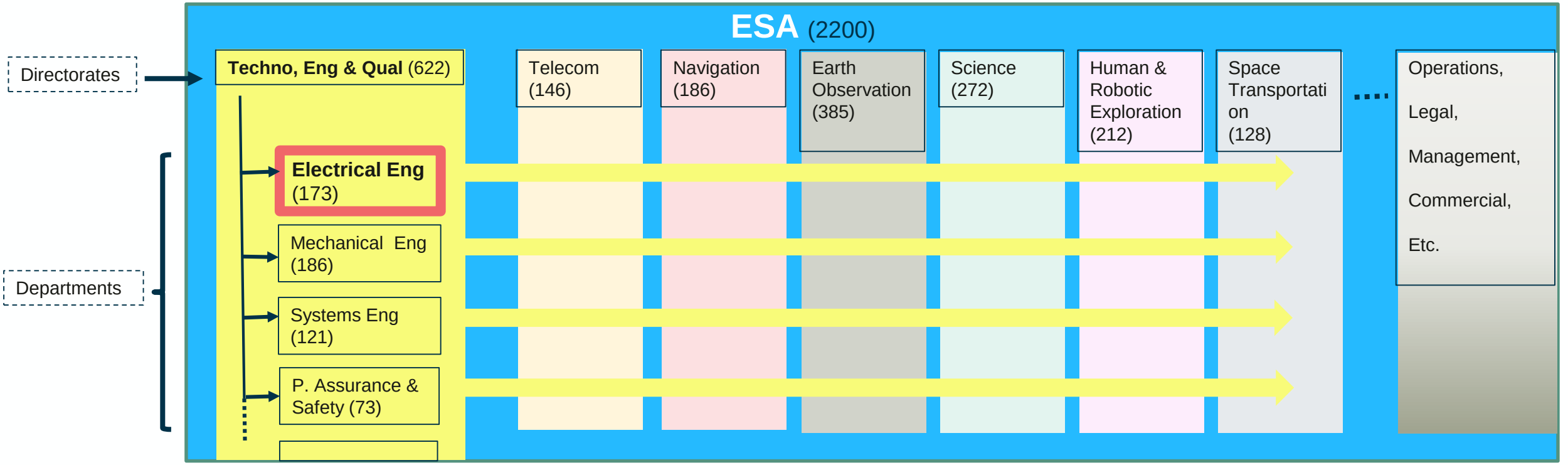
Agustin Fernandez Leon

BSc. Physics (U. Complutense Madrid) , MSc. Microlectronics (NCSU, Raleigh)

9 years at **Alcatel Telecom** (Madrid), digital ASIC designer for wireline systems

22 years at **ESA/ESTEC** (Netherlands), Head of Microlectronics section (ASIC/FPGA/IP Cores/mP)

Lead Microelectronics Engineer if Electrical Department since Jan 2022



How to do business with ESA

BSBF2022 Procurement Handbook (ESA in pag. 19-24)

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- total budget 5.5 billion EUR / yr
- Industrial database, procurement portal, process and modalities
- Funding ‘mandatory’ and ‘optional’ funding programs
- Eligibility and evaluation criteria, geographical return policy
- Support to newcomers and SMEs (training, helpdesk, portal, events)
- Technology Transfer Program

esa-star

Mandatory to register to do business with ESA , to bid for future tenders https://esastar-emr.sso.esa.int/

to see tenders / publish proposals https://esastar-publication-ext.sso.esa.int/

to find partners https://esastar-esamatch-ext.sso.esa.int/

ESA Tenders visible in esa-star

– some statistics of October 2022

1738 in total , “active” ESA tender actions (all ESA programs/budget lines, all topics)

A fraction of those (~**100**) relate to instrumentation, control and data processing systems and microelectronics building blocks. This can be explored by using filters of **esa-star tool**:

- by key words
- groups of technologies
- groups of products.

12406 companies registered (to search for matches, partners): can filter by countries, product/technology competences/key words

ESA business in data-handling and control systems

Search in *esa-star* publications by **PRODUCTS** or by TECHNOLOGY Keywords

1 - Launchers

2 - Satellites & Probes

3 - Transportation & Re-entry S

4 - Ground Segment

5 - Non Space Procurement/Se

A - AOCS & GNC
B - Electronics
C - Materials
D - Mechanisms
E - On-board SW
F - On-board Data Management
G - Optical Communication
H - Parts
I - Payloads / Instruments
J - Power
K - Propulsion
L - RF / Microwave Communi
M - System Engineering Softw
N - Structures
O - Thermal Control
P - Other

1 - On Board Data Management
- a - Central **Data Management Units** (CDMU) or Satellite Management Units (SMU)
- b - **Payload Data Handling Units**
- c - Onboard Storage (Mass Memories, Safeguard Memories)
- d - Telemetry and Telecommand Units
- e - Reconfiguration Units
- f - Remote Terminal Units
- g - Other

1.1 - On Board Data Management – BB
- a - General Purpose **Microprocessors** (ERC32, Leon 2)
- b - General Purpose **Digital Signal Processors** (e.g ADSP 21020, TMS320xx)
- c - **Microcontrollers**
- d - Dedicated **Signal Processing Processors** (e.g. FFT, Compression)
- e - General Purpose **Programable Logic** (PLD, FPGA)
- f - Rad Hard Memory
- g - High Density Memory Devices (e.g stacked SDRAM, FLASH)
- h - **Onboard Communcation** (MIL-STD-1553, CAN, SpW, Sensor Bus, Wireless)
- i - TM/TC (Formater, encryption)
- j - Other

ESA business in data-handling and control systems

Search in *esa-star* by PRODUCTS or by **TECHNOLOGY** groups

1 - Onboard Data Systems

2 - Space System Software

3 - Spacecraft Electrical Power

…

5 - Space System Control

6 - RF Systems, Payloads and Technologies

…

9 - Mission Operation and Ground Data Systems

10 - Flight Dynamics and GNSS

…

12 - Ground Station Systems and Networks

13 - Automation, Telepresence & Robotics

…

19 - Propulsion

20 - Structures

21 - Thermal

22 - Environmental Control & Life Support (ECLS) and In Situ Resource Utilisation (ISRU)

23 - EEE Components and Quality

24 - Materials and Processes

25 - Quality, Dependability and Safety

26 - OTHERS

A - Payload Data Processing
- I - System Technologies for Payload Data Processing
- II - Hardware Technologies for Payload Data Processing
- III - Software Technologies for Payload Data Processing

B - Onboard Data Management
- I - System
- II - Onboard Computers
- III - Data Storage
- IV - Onboard Networks and Control/Monitoring

C - Microelectronics for Digital and Analogue Applications
- I - Methodologies
- II - Digital and Analogue Devices and Technologies

ESA Contracts related to data handling / control systems and building blocks – statistics in September 2022

Running or soon to start activities in the **Electrical Department** of the **Technology, Engineering and Quality Directorate** of ESA/ESTEC

Topic group (ESA Electrical Department section code)	# of contracts	Total Budget (M€)	Av. Budget per contract (K€)
On-board computers & Data Handling (EDD)	62	31.00	500
ASIC, MPU/MCU, Mixed-signal standard ICs, FPGA, IP Cores (EDM)	34	23.7	700
RF payload Eng. & Digital Equipment (EFP + EFE)	122	78.4	640
Attitude Orbit & Guidance Navigation Control systems (SAS + SAG + SAA)	79	24.6	311
TOTAL	**297**	**157.7**	**530**

there are many **more activities run from the program directorates (Telecommunication, Earth Observation, Navigation, Science, Human and Robotic Exploration and Space Transportation)** where data handling and control systems are developed for specific platforms and instruments of satellites, probes, rovers, launchers or experiments aboard the International Space Station.

ESA Contracts related to data handling / control systems and building blocks – statistics in September 2022

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TOTAL	**297**	**157.7**	**530**

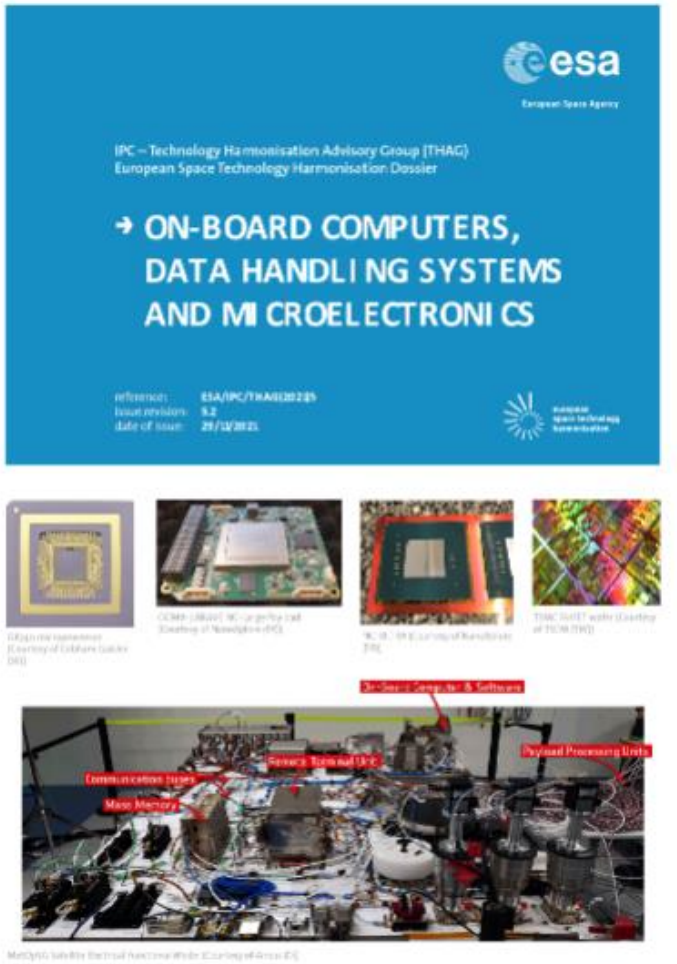
From now on this presentation focuses on these technology areas, and the activities running and proposed by those groups of ESA experts

Future plans for On-board Computers (OBC), Data Handling Systems (DHS) and Microelectronics

ESA periodically (every 2-3 yrs) releases a “technology harmonization dossier” that summarises state-of-the-art, trends, market analysis, project needs and roadmaps including recently closed, running and **proposed new activities (in next 5 years)**.

Last “**OBCDHSM** dossier” release: 29 Nov 2021

“TECHNOLOGY HARMONISATION DOSSIER - ON-BOARD COMPUTERS , DATA HANDLING S YSTEMS AND MICROELECTRONICS“ - ESA/IPC/THAG(2021)5



130 new proposed activities -> 104M€ (average 800K€ per activity)

131 running activities or approved activities -> 116.7 M€

All European space sector stakeholders can request access to the Harmonisation Document Management System (HDMS/DCCM: https://tec-polaris.esa.int/eclipse) by sending an e-mail to harmo@esa.int providing business affiliation and position in the company. https://www.esa.int/Enabling_Support/Space_Engineering_Technology/Technology_Harmonisation

Past tenders, Future tenders & budget estimations

As stated in “On-Board Computers, Data Handling Systems And Microelectronics” dossier, Nov 2021

2016-2020

Estimation of total budget spent **8.7 M€ / year**

2021-2026

130 “new proposed” activities -> 104M€

average per activity -> 800K€

131 “already running” and “approved” activities -> 116.7 M€

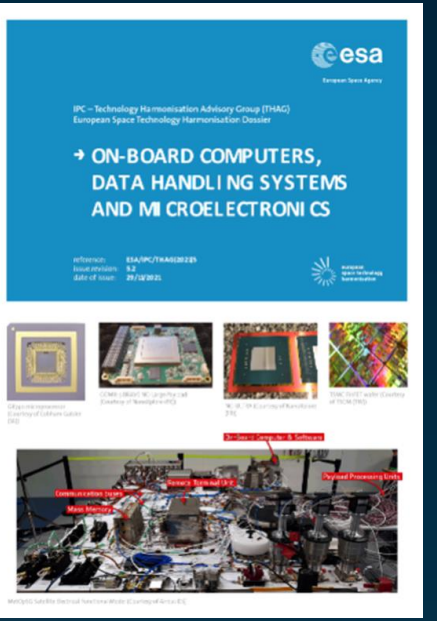
Past tenders, Future tenders & budget estimations

Important to know

- **Not all proposed activities get approved and funded!**
- **There is ESA internal competition - more activity proposals than ESA budget available.**
- **Many ESA funding programs available, targeting different Technology Readiness Levels, application domains, “mandatory” and “optional” (which require national ESA delegation support and industry co-funding)**
- **Some ESA proposed technology developments also receive support from other EU institutions (e.g. EC, EDA, CERN) and national agencies and programs, and ESA coordinates with them.**
- **ESA technology harmonization dossiers do not freeze work plans nor guarantee funding.**
- **New activities are often proposed in between dossier releases, some get cancelled or superseded.**

On-Board Computers, Data Handling Systems and Microelectronics (OBCDHSM) technology harmonization dossier

The new THD dossier OBCDHSM contains detailed State-of-the-Art, Trends and activity Roadmaps



Technology overview and trends organized in 3 technology families

- Technology Family 1: CDHS Architecture, units, modules and communication systems
- Technology Family 2: Microelectronic devices and enabling technology
- Technology Family 3: CDHS EGSEs & Microelectronics Development methods and tools

The objectives and roadmaps have been organized in 10 “AIMs” with a top-down approach from DHS architecture down to microelectronics.

Technical Perimeter of the OBCDHSM Dossier

Technology Family 1: Computer Data Handling System (CDHS) Architecture, units, modules and communication systems

- Platform and Payload CDHS Architectures Background
- CDHS Units, Modules and functions (Platform and Payload)
- CDHS communication links, buses and networks

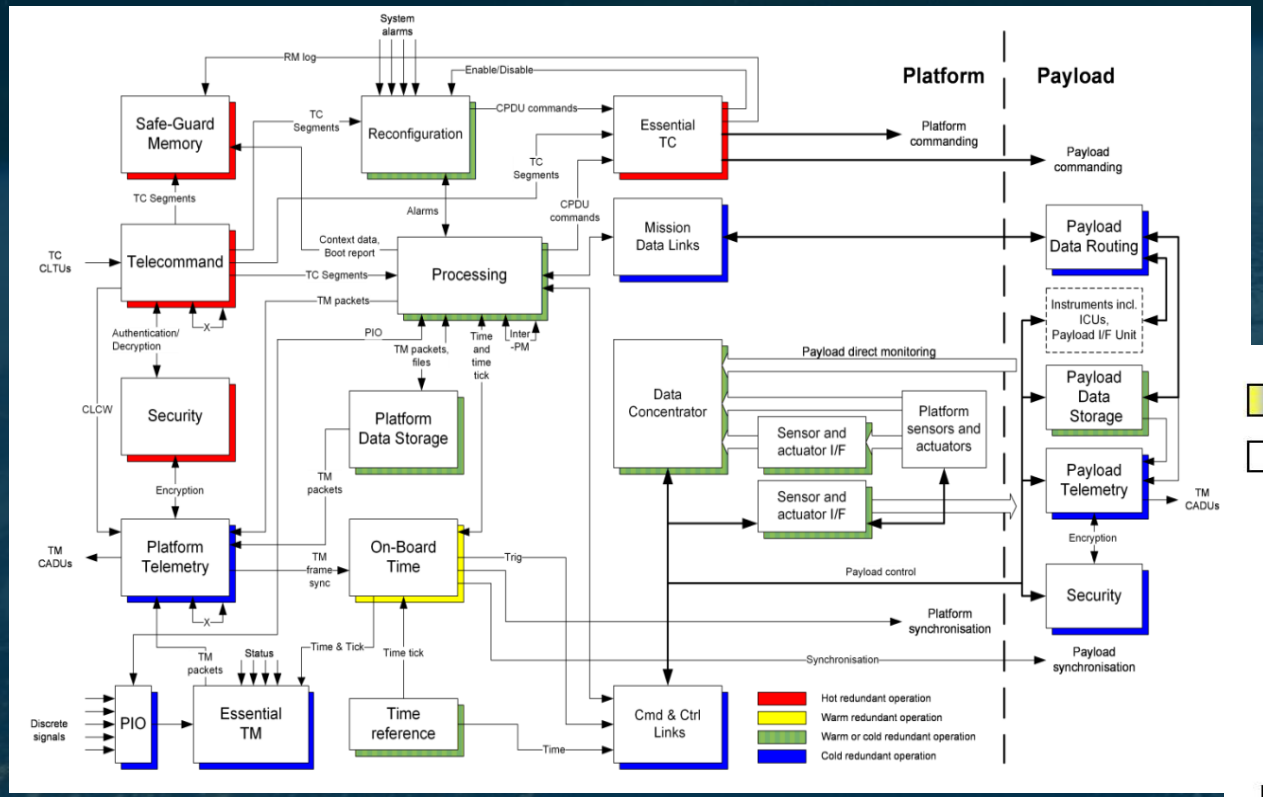
Technology Family 2: Microelectronic devices and enabling technology

- FPGA (Field Programmable Gate Array)
- Microprocessors, microcontrollers, DSP
- ASSP (Application Specific Standard Products) (digital, analogue and mixed-signal)
- ASIC (Application Specific Integrated Circuit) platforms (rad hard cell libraries, IP, Design Kits, packaging, supply chain space quality)
- IP (Intellectual Property) Cores

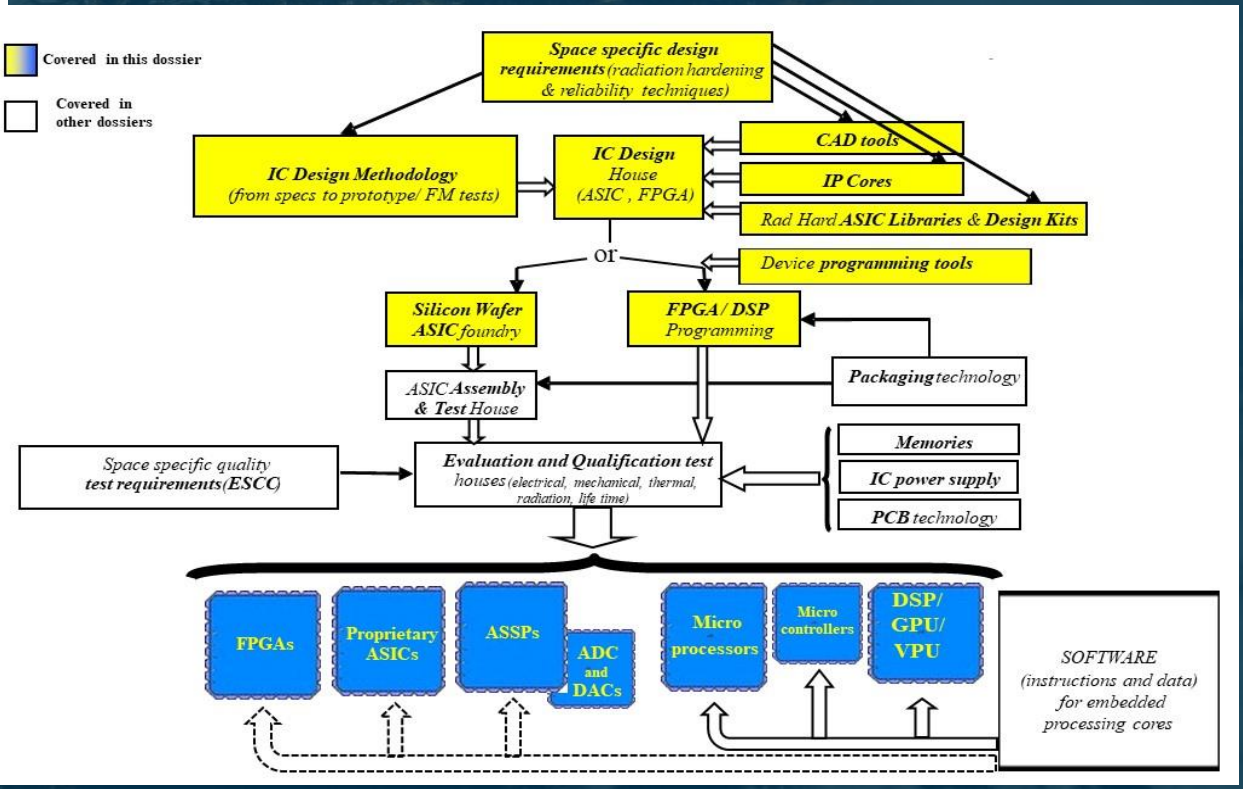
Technology Family 3: CDHS EGSE (Electrical Ground Support Equipment) & Microelectronics Development methods and tools

- EGSE and tools for CDHS used at satellite level or instrument level
- EGSE for CDHS Units
- EGSE that are used to verify the proper functionality of a module to be then integrated in a CDHS unit.
- Microelectronics development methods and tools

Technical Perimeter of the OBCDHSM Dossier

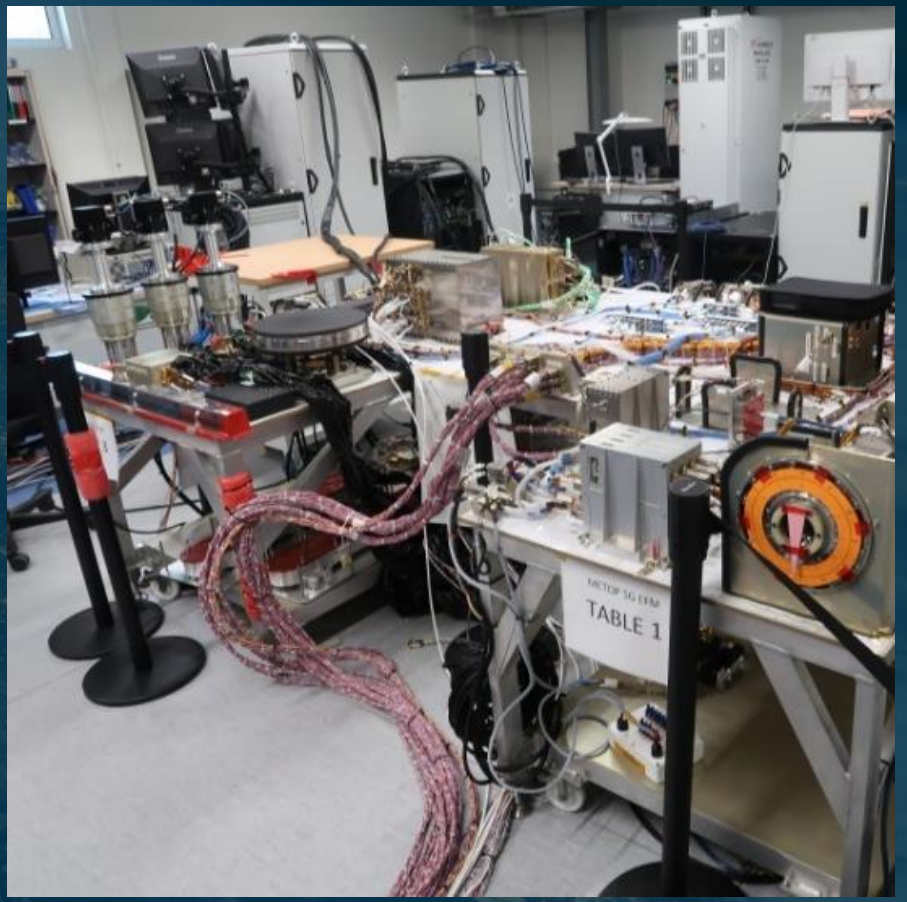


SAVOIR
space avionics open interface architecture



AIMS overview: grouping activity proposals, top-down

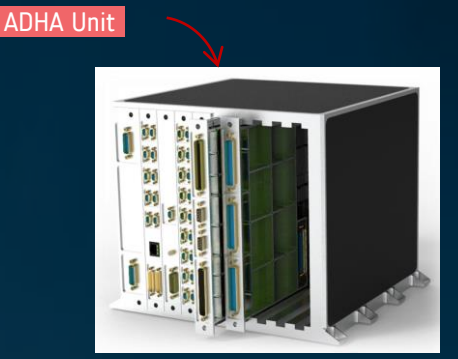
1. AIM A Define and adopt unified OBCDH architectures based on modules
2. AIM B Design, develop, manufacture and qualify buses, network and communication technologies
3. AIM C Design, develop, manufacture and qualify OBCDH modules (including AI, ML and rad-hard components and COTS with radiation mitigation)
4. AIM D Develop Building Blocks to support OBCDH modules development
5. AIM E Develop EGSE to support the test and integration of OBCDH units/modules
6. AIM F Enhance characteristics/functions of current ASIC Platforms and develop new Ultra Deep Sub-micron (UDSM) ASIC Platforms
7. AIM G Improve and expand the European rad-hard FPGA family
8. AIM H Improve and expand the European rad-hard Microprocessors, Microcontrollers and DSPs
9. AIM I Improve and expand the European rad-hard Application Specific Standard Products (ASSPs) family
10. AIM J Improve and expand the European IP Cores catalogue and respective Design Methods and Tools



AIM A: Define and adopt unified OBCDH architectures based on modules

Objective:

Provide modular and standardized HW architectures for AVIONICS and PAYLOAD data handling in order to improve interoperability, flexibility, scalability, competitiveness and ease the procurement.



Key Future Activities

- Advanced Data Handling Architecture. Incremental building approach with:
  - Architecture consolidation and documentation preparation (2022)
  - First EM unit (2023) and then EQM unit (2025)
- OBCDHS architectures study for high reliability (2FT) missions types.
- Study of OBCDHS architectures based on microcontrollers (decentralized DHS Architectures)

2 running activities,
2 M€

5 proposed activities,
16.75 M€

AIM B: Design, develop, manufacture and qualify buses, network and communication technologies

Objective:

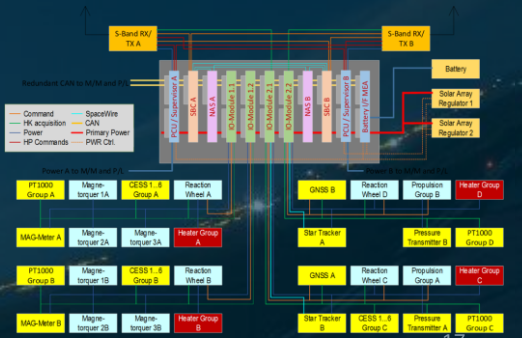
- To endorse the usage of standardized protocols (CAN-Bus, MIL-Bus, SpaceWire, SpaceFibre, TTEthernet).
- To develop new qualified network components (end points, routers etc.) to ease integration, reduce development time and costs, and increase performance.
- To promote best practices for verification and validation (e.g. network simulation, physical testing).
- To continuously improve communication buses (incl. protocols) for better usability, reliability, and performance.

Key Future Activities:

- SpaceWire: Deterministic communication (new routing switch), network management, network simulators
- SpaceFibre: Interface chip, routing switch chip, physical layer testing, reference designs
- Ethernet: TTEthernet test bed, end point, and switch; Time Sensitive Network characterization and development
- CAN: Integrated design environment for CAN-based networks

12 running activities,
4.6 M€

14 proposed activities,
5.4 M€



AIM C: Design, develop, manufacture and qualify OBCDH modules

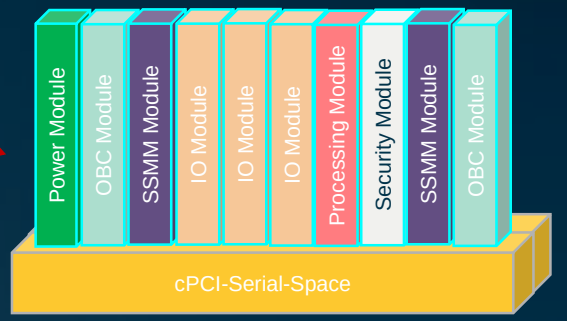
Objective:

Develop a portfolio of OBCDHS modules that can:

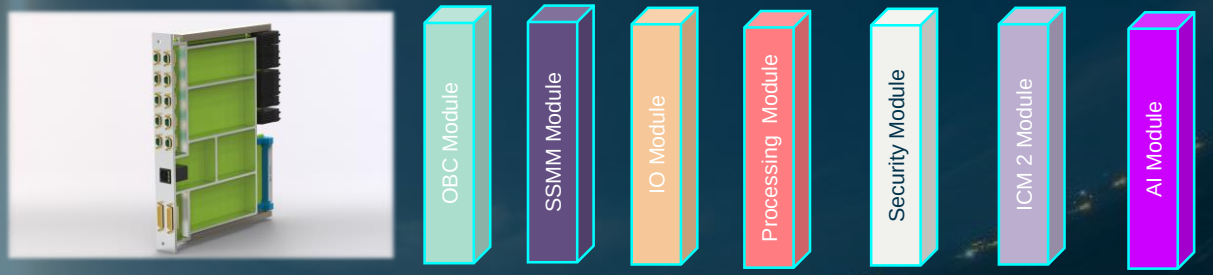
- be rapidly implemented in a standardized OBCDHS Architecture (AIM A)
- increase On-Board Processing capability (Processing Modules (HW/SW) & tools).
- support disruptive data analysis technologies (AI/ML) for supporting avionics and payload applications (incl. data compression and reduction).

Key Future Activities

- HW Processing Modules based on rad-hard Microelectronics (under development by primes, with European processors and FPGAs)
- HW Processing Modules based on COTS
- Cubesat Modules
- ADHA Modules (EM)



ADHA Modules



21 running activities,
15.1 M€

19 proposed activities,
12.7 M€

AIM D: Develop Building Blocks to support OBCDH modules development

Objective:

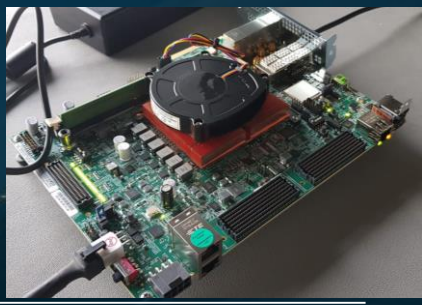
Develop a portfolio of building blocks techniques to support and ease OBCDHS modules developments

Key Activities:

- COTS activities: selection, characterization, design mitigation techniques, robustness and performance evaluation.
- Component benchmark activities (OBPMark completion, FPGA / GPU / Accelerators).
- Machine Learning investigations: evaluation & assessment of specific techniques on different HW platforms (NN, Neural Morphic, …)
- Algorithms and relevant datasets (image/video/data compression, data reduction, cloud detection, etc.)

4 running activities,
2.8 M€

33 proposed activities,
12.5 M€



AIM E: Develop EGSE for OBCDH units/modules

Objective:

Develop EGSEs to support the test, integration and verification of OBCDH units/modules and benefit of synergies and commonalities.

Key Future Activities:

- EGSE to test buses, network and communication technologies (SpaceWire, SpaceFibre, Ethernet, TSN, CAN): network simulators, physical layer testing, test bed, bus tester.
- ADHA module crates or racks
- ADHA unit EGSE (incremental approach following the ADHA modularity)

1 running activity,
220 k€

3 proposed activities,
1.6 M€

AIM F: Enhance characteristics/functions of current ASIC Platforms and develop Ultra Deep Sub-Micron ASIC Platforms

Running evaluation/consolidation activities on several ASIC manufacturing processes and design kits:

12 nm FinFET (GF) - customer chip & IP eval

16 nm FinFET (TSMC) - test chip & IP eval + simulations

22 nm planar FDSOI (GF) - customer chip & test chip & IP eval

65 nm (TSMC & IMEC DK) - customer chip & test chip & IP eval

28 nm & 65 nm (ST) - customer chip eval

150 nm SOI (UMC & MCHP DK, LFoundry & RedCat) - customer chip & test chip & IP eval

180 nm (XFab, UMC & IMEC DK) - customer chip & test chip & IP eval

7 running activities,
14 M€ (ESA 7.7M€ + 6.2M€ European Commission)

6 proposed activities,
12.4 M€

proposed

6 nm FinFET (TSMC) - test chip & IP eval + simulations

Further development and consolidation of Design Kits and rad hard IP for the various platforms, for high speed digital processing and data communication, detector back-ends, power conversion and control,

AIM G: Improve and expand the European rad-hard FPGA family

Running

European rad-hard FPGA family development and qualification:

>> NanoXplore NG-Medium (65nm), Large, Ultra & Ultra300 (28nm), Ultra6 (6nm)

>> NanoXmap programming tools

Mitigation techniques for complex COTS FPGAs

Reliability evaluation of complex COTS FPGAs

Reliable reconfiguration of FPGAs on-board

15 running activities, 31M€ (ESA 7.6M€ + 13M€ EC + 10.4M€ national prog)

4 proposed activities, 1.5 M€

proposed

Evaluation and demos of embedded FPGA IPs and tools

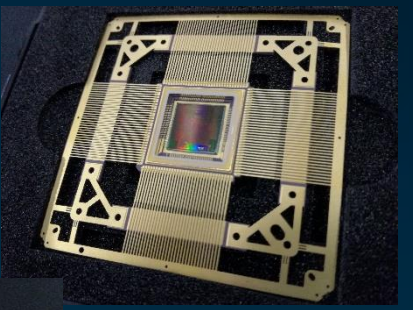
More evaluations of non-European reprogrammable FPGAs (e.g. Microchip PolarFire, Xilinx KU060)

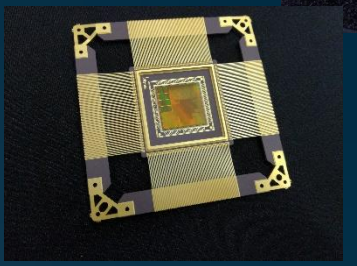
AIM H: Improve and expand the European rad-hard Microprocessors, Microcontrollers and DSPs

Running

European rad-hard microprocessors and microcontrollers development and qualification:

- >> based on LEON (SPARC) - Cobham Gaisler GR740 (LEON4), GR765 (LEON5)
- >> based on RISC-V - Cobham Gaisler GR7xV(RISC-V)
- >> based on ARM – Microchip SAM radiation hard and tolerant microcontrollers
- >> other processor cores (e.g. DPC TAS-BE, MORAL IHP Peaktop)





proposed

RISC-V instruction extensions, SW tool ecosystem

RISC-V Fifth Generation Space Microprocessor (VGSM) EM and FM

Next generation ARM MCU (55nm) and MPU (28nm)

Space Microcontroller with open instruction set architecture

14 running activities, 14.2M€ (ESA 9.1M€ + 3M€ EC + 2.1M€ national prog)

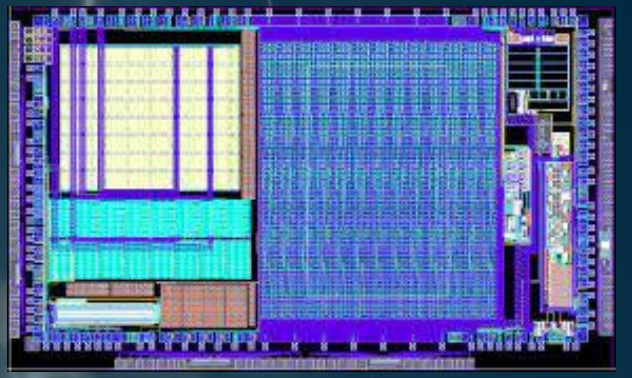
4 proposed activities, 6.9 M€

AIM I Improve and expand the European rad-hard ASSP family

Running

European rad-hard Application Specific Standard Products (ASSP) development and qualification:

- >> Latch-up protection
- >> ADC, DAC
- >> electro-optical transceivers
- >> power conversion, conditioning and control
- >> LVDS drivers/receivers
- >> evaluation of non volatile memories
- >> frequency synthesizers
- >> high speed communication interfaces and switches (e.g. SpaceFiber chips)
- >> Telecommand and Telemetry encoder/decoder chips



27 running activities, 21.7 M€ (ESA 13.1M€ + 7.2 M€ EC + 1.4 M€ national prog)

proposed

New developments on above applications, evaluations (also of COTS), qualifications

22 proposed activities, 28.7 M€

AIM J: Improve and expand the European IP Cores catalogue and respective Design Methods and Tools

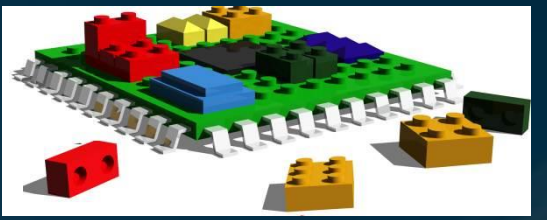
Running

ESA IP Cores catalogue maintenance and expansion (e.g. CCSDS data compression and optical data TX, LEON ISA extensions, ADC, ADPLL)

Universal VHDL Verification Methodology (UVVM) and tools

HW-SW co-design virtual platforms and demos (e.g. TERMA SkyRocket)

Functional and rad characterisation of COTS components



proposed

AI with FPGAs (IPs and tools)

New IP Cores (AMBA to AXI bridge, supervisors for COTS devices, RISC-V extensions, high speed communications, DSP accelerators, ADHA functions/interfaces, TSN, TTEthernet, etc.)

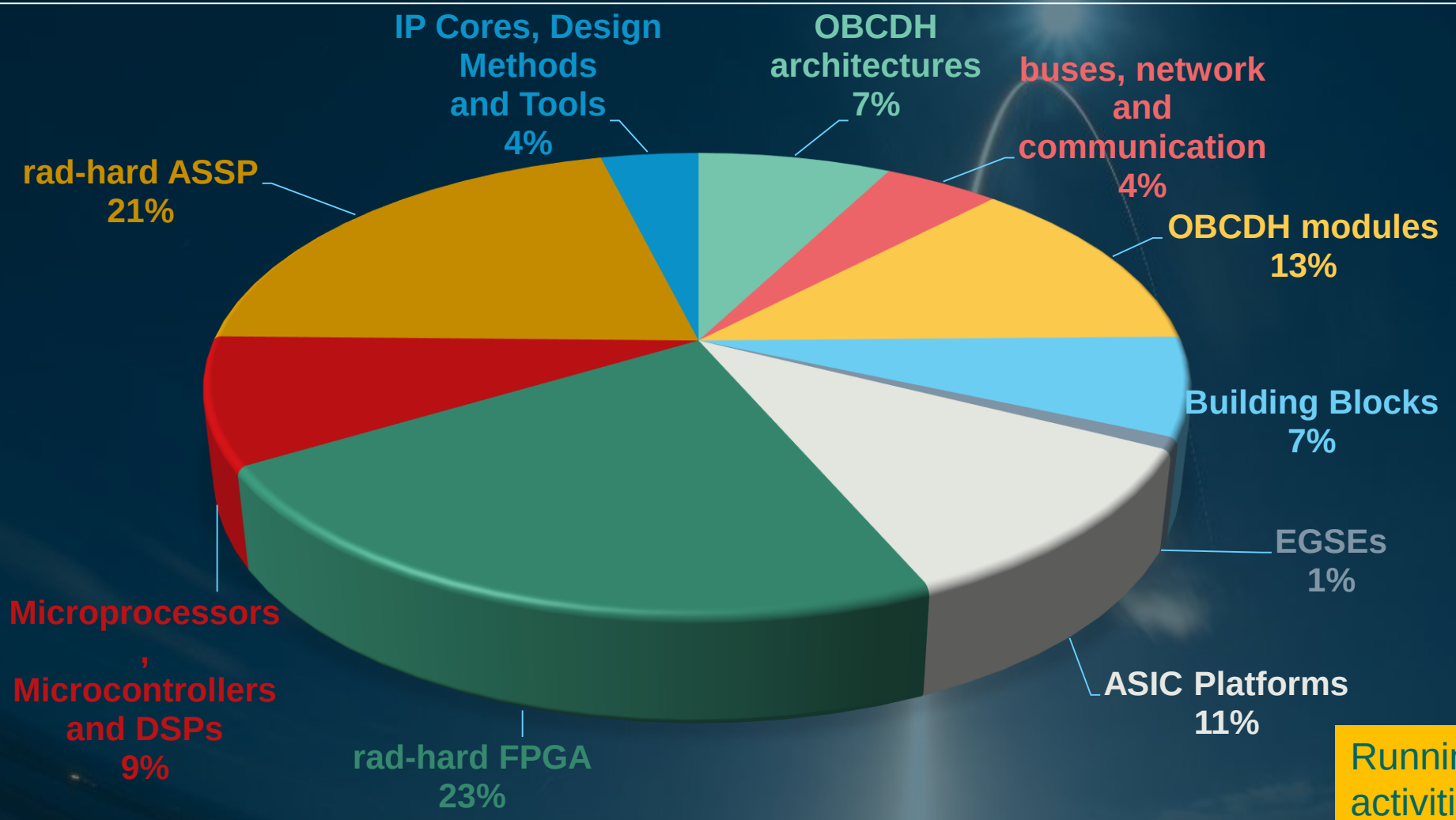
Validation tests functional coverage methods and tools

Radiation effects mitigation techniques for COTS and rad tolerant (non rad hard) FPGAs

16 running activities, 3.6 M€ (ESA)

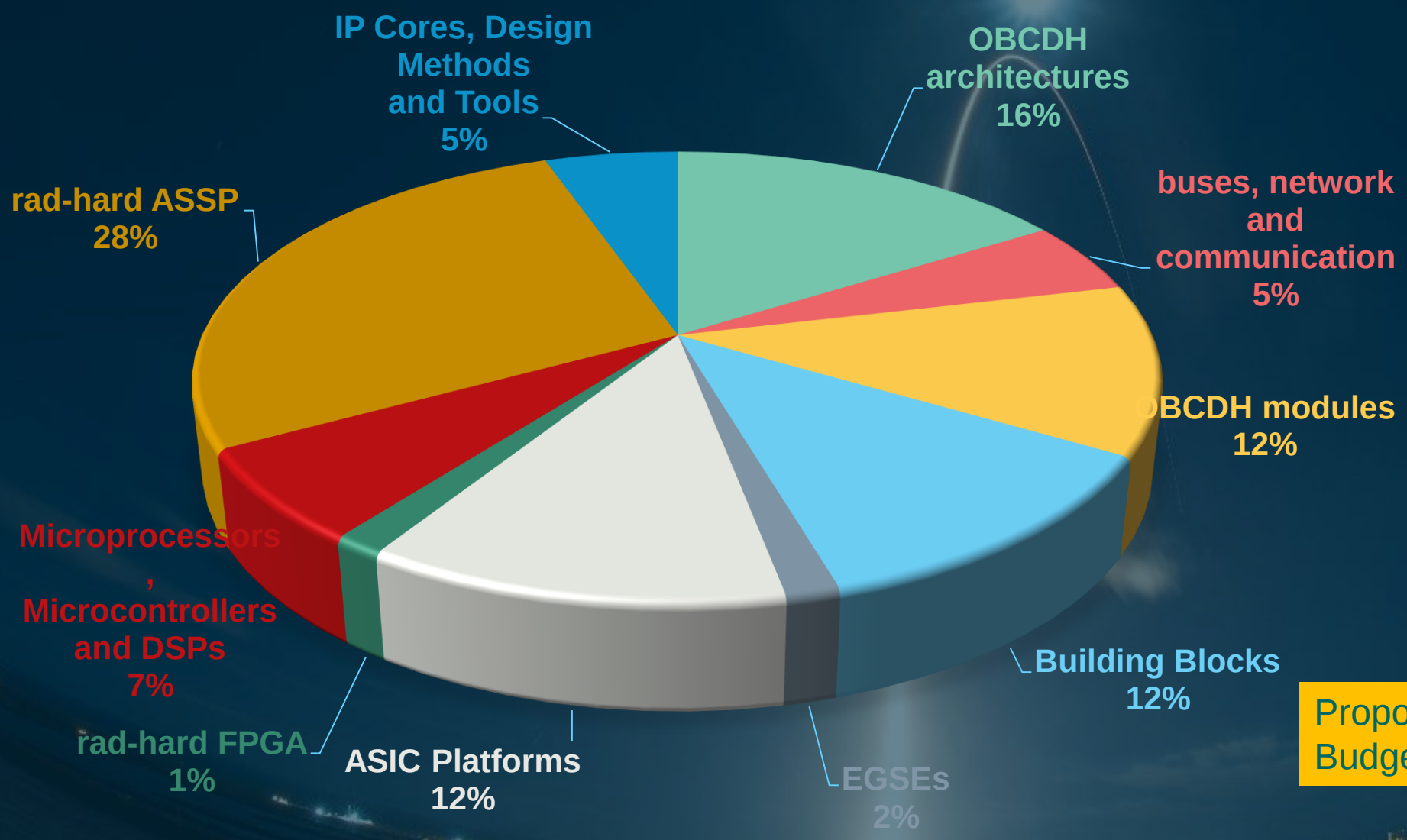
17 proposed activities, 5.5 M€

Budget: Running and Proposed Activities



Running and Proposed activities: Total Budget of **220.7 M€**

Budget: Proposed Activities



Proposed activities: Total Budget of **104 M€**

Expected tendering volume

2022 - 2027	Data handling and control			
	Electrical systems		Microelectronics	
	Total budget M€	# tenders	Total budget M€	# tenders
OBCDHS architectures based on modules	16.75	5		
Buses, network and communication	5.4	14		
OBCDHS modules	12.7	19		
Building blocks for OBCDHS modules	12.5	33		
EGSE for OBCDHS units/modules	1.6	3		
ASIC Platforms, UDSM			12.4	6
FPGA			1.5	4
Microprocessors, microcontrollers			6.9	4
Mixed-signal ASSPs			28.7	22
IP Cores, design tools			5.5	17
TOTALS	**48.95 M€**	**74**	**55 M€**	**53**

Seeking more ESA resources for European EEE critical space components

ESA is coordinating the definition of future activities and a request for additional funding to ESA delegations at November 2022 ESA Ministerial Council, under an initiative called

“EEE European Components Sovereignty for Space”

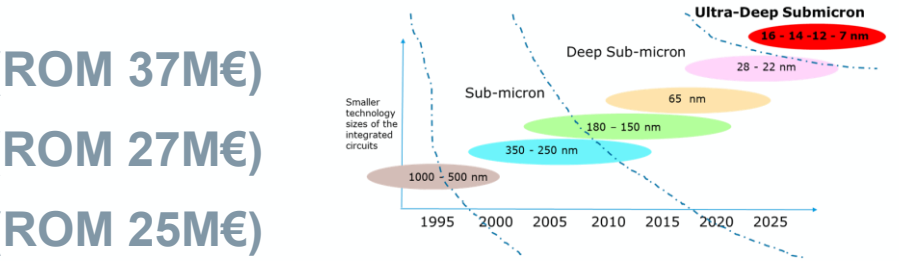
Amongst others (e.g. GaN/SiC, solar cells, PCB/packaging, test facilities , it focuses on these important areas:

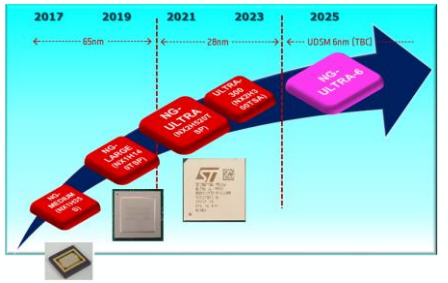
“Ultra Deep Sub-Micron (UDSM) radiation hard components technology”

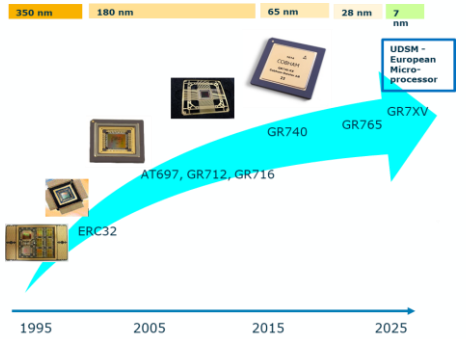
-UDSM ASIC platform (ROM 37M€)

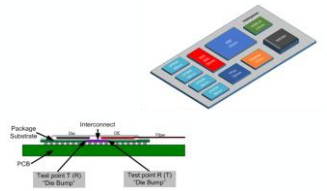
-UDSM FPGA (ROM 27M€)

-UDSM Microprocessor (ROM 25M€)









If successful, it will be funded as part of an ESA “optional” program: ESA - About the General Support Technology Programme (GSTP)

Key technology challenges of OBC, Data Handling and Microelectronics building blocks for space applications

- Advanced Data Handling Architecture (**ADHA**) based on **interchangeable and interoperable** standardized modules.
- **Higher integration** of OBC facilitated by **multi-core System-on-Chip** and processors.
- Reduced and **standardized interfaces of I/O modules** for Remote Terminal Units and Instrument Control Units.
- Instrument **advanced computing & processing** modules incl. **AI** and **ML** applications.
- Availability of **European radiation hard microchips**: ASIC tech platforms (**ultra deep submicron**), **FPGA**s, **Microprocessors and Microcontrollers**, **Application Specific Standard Products** (converters, front ends, High Speed Serial Links), Digital and Analogue **IP Cores**.
- Heterogeneous integration multi-die packaging solutions (custom **System-in-Package, 2.5/3D, "chiplets"**)
- Evaluation & **mitigation techniques** for reliable use of high performance **COTS** and **rad tolerant** microelectronic devices
- **European Non-Dependence**

Thanks for your attention!

Questions?

More info:

OBCDHSM dossier:

https://www.esa.int/Enabling_Support/Space_Engineering_Technology/Technology_Harmonisation

ESA optional technology program (GSTP):

https://www.esa.int/Enabling_Support/Space_Engineering_Technology/Shaping_the_Future/About_the_General_Support_Technology_Programme_GSTP#:~:text=What%20is%20GSTP%3F%20Through%20the%20optional%20General%20Support,concepts%20into%20a%20broad%20spectrum%20of%20useable%20products.

esa-star procurement platform

to register for future tenders https://esastar-emr.sso.esa.int/

to see tenders / publish proposals https://esastar-publication-ext.sso.esa.int/

to find partners https://esastar-esamatch-ext.sso.esa.int/

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