COMPANY OVERVIEW

June 2022

E4 IN A NUTSHELL

20 YEARS ANNIVERSARY
2002 - 2022

WHO WE ARE

E4 Computer Engineering designs and manufactures highly technological solutions for HPC Clusters, Cloud, Data Analytics, Artificial Intelligence and Hyper-Converged infrastructure for the Academic and Industrial markets. We have been collaborating for years with the main research centers at national and international level (Cineca, CERN, ECMWF, LEONARDO) and we are involved in national and European projects in the HPC and AI fields (EuroHPC JU EPI, EUPEX, Horizon Europe)

VISION

We explore future scenarios to find solutions for highly performing computational needs in application areas that are unimaginable today.

MISSION

We anticipate the ever-accelerating disruptive transformation of our era, providing mature solutions in sophisticated technological contexts with a dizzyingly innovative approach

APPROACH

Each E4 solution is UNIQUE, like each of our customers; TESTED in every single component; VALIDATED to verify the actual performance of each system and SERVED by technicians who provide assistance in the most extensive and complex Italian and European computing infrastructures.

ISO 9001:2015 ISO 14001:2015

E4 HISTORY

2002

2005
FIRST INFINIBAND CLUSTER

2009
FIRST GPU CLUSTER

2012
SGI ITALIA ACQUISITION

2013
FIRST ARM+GPU SERVER AND FIRST ARM CLUSTER

2016-2017
FIRST OPENPOWER SERVER & PETAFLOPS CLUSTER

299° IN TOP500 (JUNE 2017)
14° IN GREEN500 (JUNE 2017)

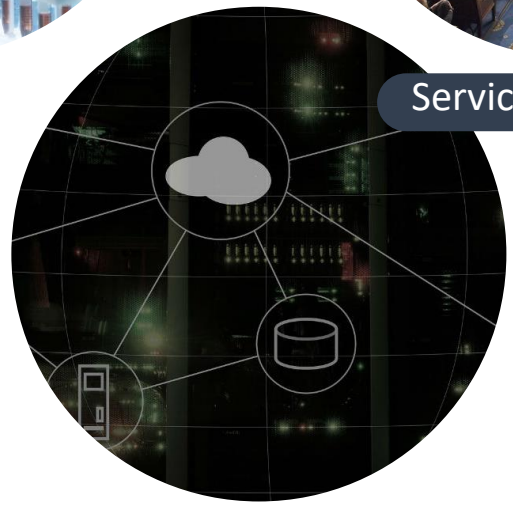
2018
E4 ANALYTICS FOUNDATION

2019
SW INTEGRATION & CI/CD FACTORY

2021
INTERNATIONALIZATION PLAN BEGINS WITH E4 DEUTSCHLAND

2022
BOLOGNA TECNOPOLO (ATOS ENGAGEMENT)

WHERE WE SERVE



E4 APPLICATION / SW STACK

High Performance Computing

GPU for Artificial Intelligence Appliance

Container Platform

High Performance Cloud

VSTONE

Converged Virtualization

VSHUFFLE

Hyperconverged Virtualization

TWINSTONE

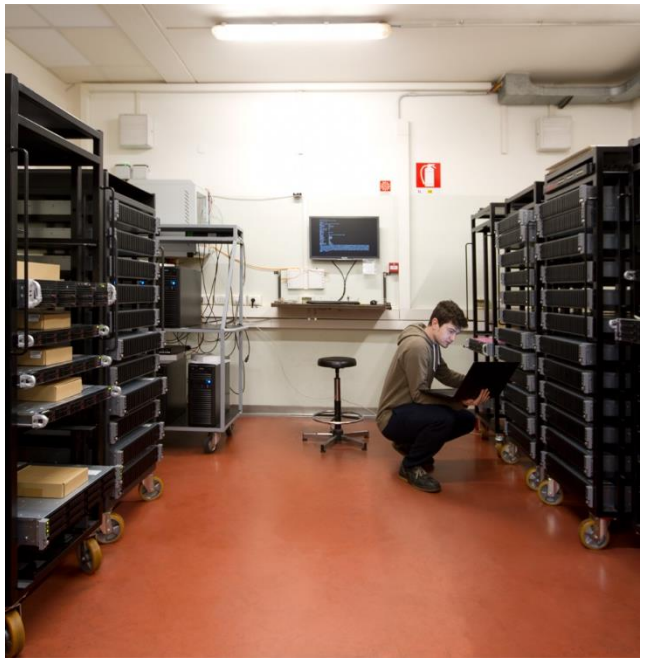
Virtualization Backup & DR Solution

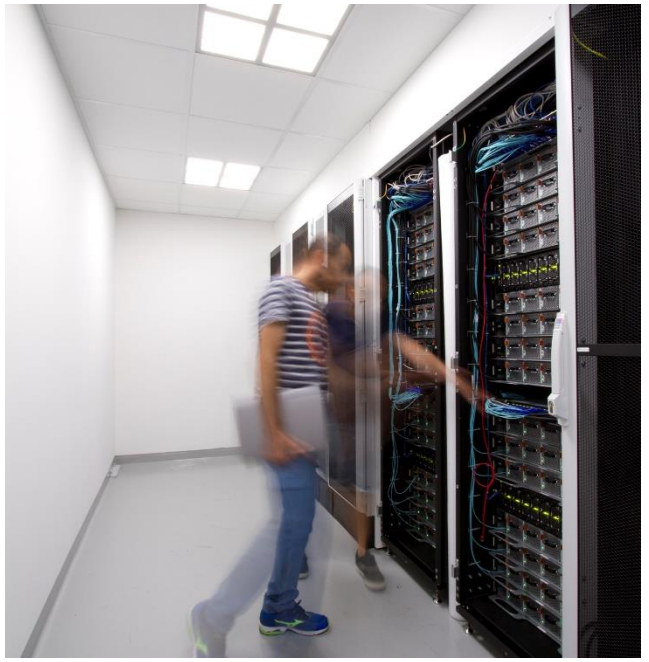
E4 SOLUTIONS AT A GLANCE

- Standard Solutions
- Application / SW Stack
- Prototypes
- Talor-made solution upon requirements
- Standard and In-Depth Services

WHEN PERFORMANCE MATTERS

E4 TECH FACTORY





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UNIQUE like each of our customers

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VALIDATED at any level to check the actual performance of each system

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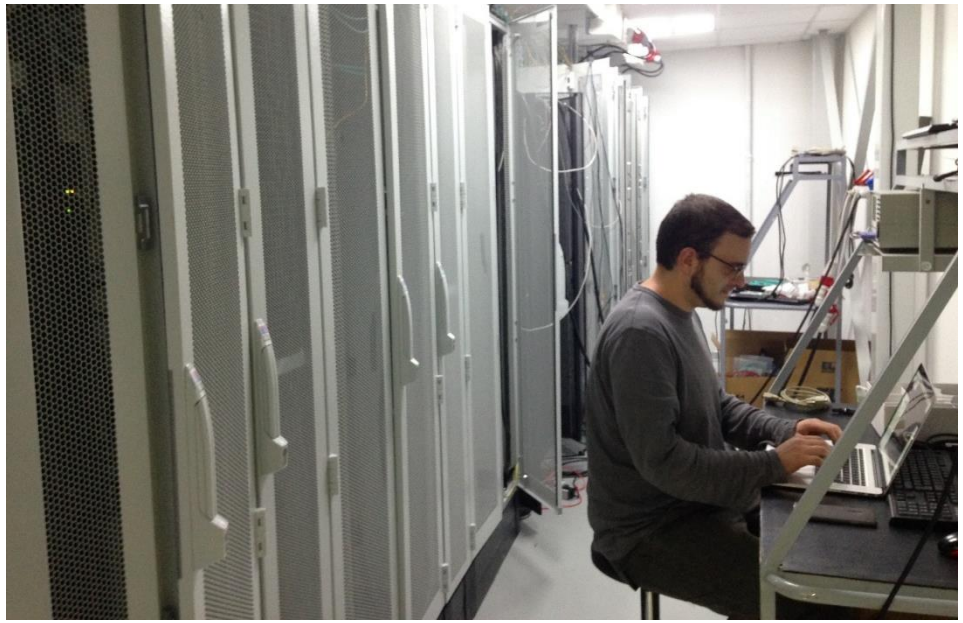
SERVED by systems engineers who operate in the most complex Italian and European computing infrastructures

E4 R&D LAB

- 30 m^2
- temperature 27/30°c
- 6 x Rack 19’

- 4 x Chiller 22 kw
- Active Power available ~100 kw
- Hardware Management via OpenDCIM open source



E4 PROTOTYPE– ARKA ARM 2013

2013

Features	**8x ARKA Blade +** X86_64 node for cross compilation
CPU	NVIDIA® Tegra® 3 ARM Cortex A9 Quad-Core
GPU	NVIDIA K20
Memory	2GB x CPU 2GB x GPU
Peak Performance	270 Single Precision GFLOPS
Network	Mellanox InfiniBand QDR
Storage	1x SATA 2.0 Connector
USB	3x USB 2.0
Display	3x HDMI + serial console available

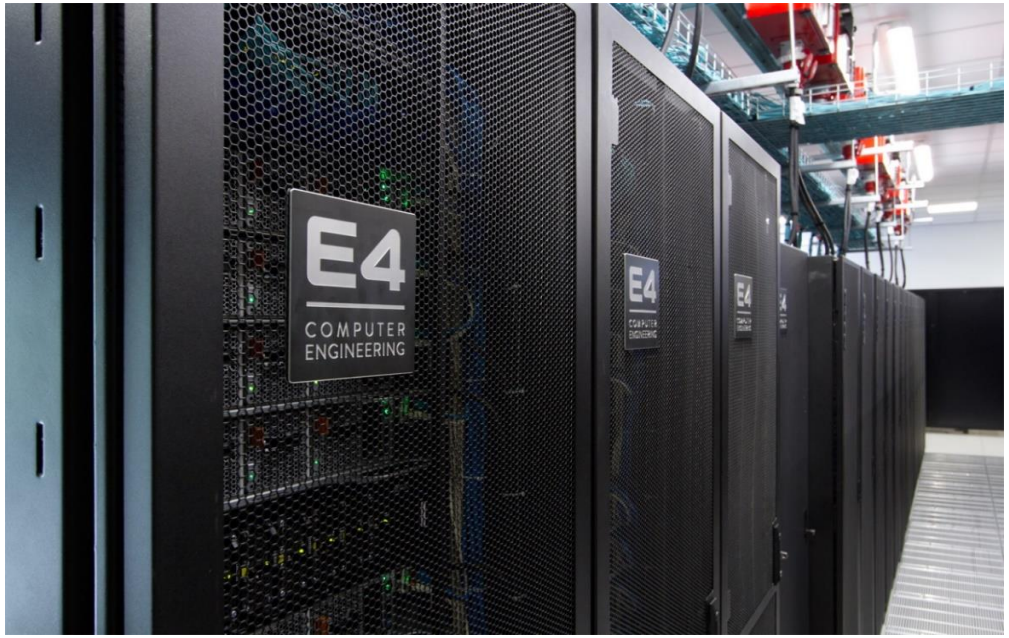
- Prototype @ ISC13
- Integrated in the Pedraforca system installed at the Barcelona Supercomputing Center
- First Arm + Infiniband + GPU cluster

E4 RK002

E4 – TAILOR MADE DESIGN AND INTEGRATION

2017

D.A.V.I.D.E. – CINECA



“Design of an Energy Aware Petaflops Class High Performance Cluster Based on Power Architecture”
978-0-7695-6149-3/17 $31.00 © 2017 IEEE
DOI 10.1109/IPDPSW.2017.22

“The D.A.V.I.D.E. Big-Data-Powered Fine-Grain Power and Performance Monitoring Support”
CF ’18, May 8–10, 2018, Ischia, Italy
© 2018 Association for Computing Machinery.
ACM ISBN 978-1-4503-5761-6/18/05. . . $15.00
https://doi.org/10.1145/3203217.3205863

D.A.V.I.D.E. – FIRST PETAFLOPS CLUSTER

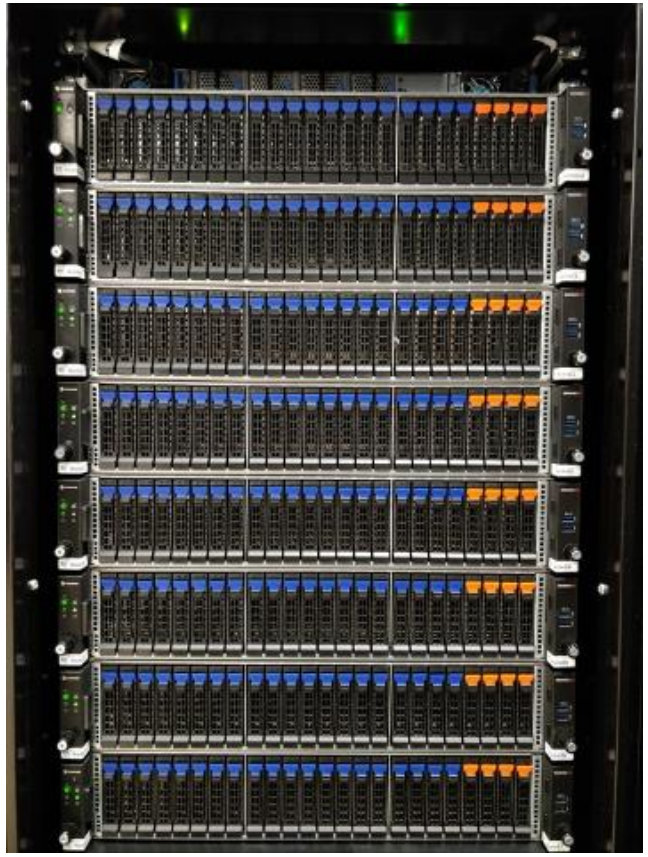
- **2 Power8 Cluster Front End in High Availability**
- **45 Computing nodes with Power 8+ Architecture to Exploit:**
  - The High Speed Bus (NVLink) between GPU-GPU and GPU-CPU
  - the Low Memory Latency and High Memory Bandwidth
- **4 Pascal P100 with NVLink per node**
  - the single link supports up to 40 GB/s of Bidirectional Bandwitdh.
  - Up to 4 links enabling an aggregate maximum bandwitdh of 160 GB/s
  - P100 performance is:
    - 5.3 Tflops in double precision floating point,
    - 10.6 Tflops in single precision and
    - 21.2 Tflops in half precision.
- **2 Mellanox EDR per node (one per CPU socket) with an aggregate bandwith per node of 200Gb/s**

299° IN TOP500 (JUNE 2017)
14° IN GREEN500 (JUNE 2017)

E4 PROTOTYPE - ARMIDA ARM TX2 BASED CLUSTER

2019

- 8 Node cluster with GPUs:
  - tlnode01.e4red is the login node
  - Tcnode0[1-7].e4red are the computing node
    - Red Hat 8, kernel 4.18.0-80
    - dual socket, 32 cores per socket with Cavium ThunderX2 processors
    - 256 GB RAM
    - connected with InfiniBand 100 Gb/s network
    - Tcnode0[5,6] with NVIDIA V100 GPUs



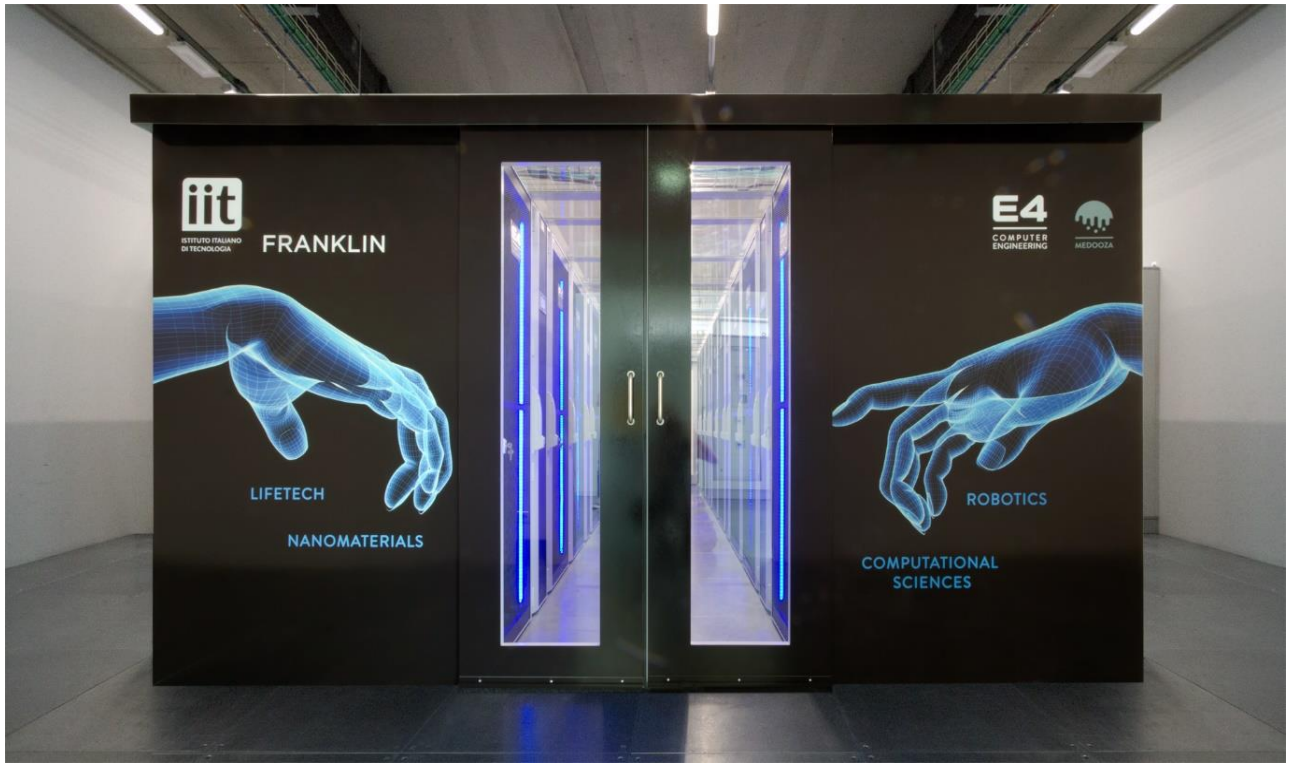
“Molecular Dynamics Performance Evaluation with Modern Computer Architecture”

@ Springer Nature Switzerland AG 2020
Y. D. Sergeyev and D. E. Kvasov (Eds.): NUMTA 2019, LNCS 11974, pp. 322–329, 2020.

https://doi.org/10.1007/978-3-030-40616-5_26

E4 – TAILOR MADE DESIGN AND INTEGRATION

2020



Istituto Italiano di Tecnologia (IIT)
Genova

E4 – SPECIAL DEPLOYMENT AND FULL RANGE SUPPORT

2021 ongoing

ECMWF – Tecnopolo di Bologna

E4 PROTOTYPE – TEXTAROSSA IDV-E ARM + FPGA + Dual Phase Liquid Cooling

2022 ongoing

"The TEXTAROSSA Approach to Thermal Control of Future HPC Systems" submitted to 22nd Samos International Conference on Enbedded Computer Systems: Architectures, Modelling and Simulations https://samos-conference.com/wp/

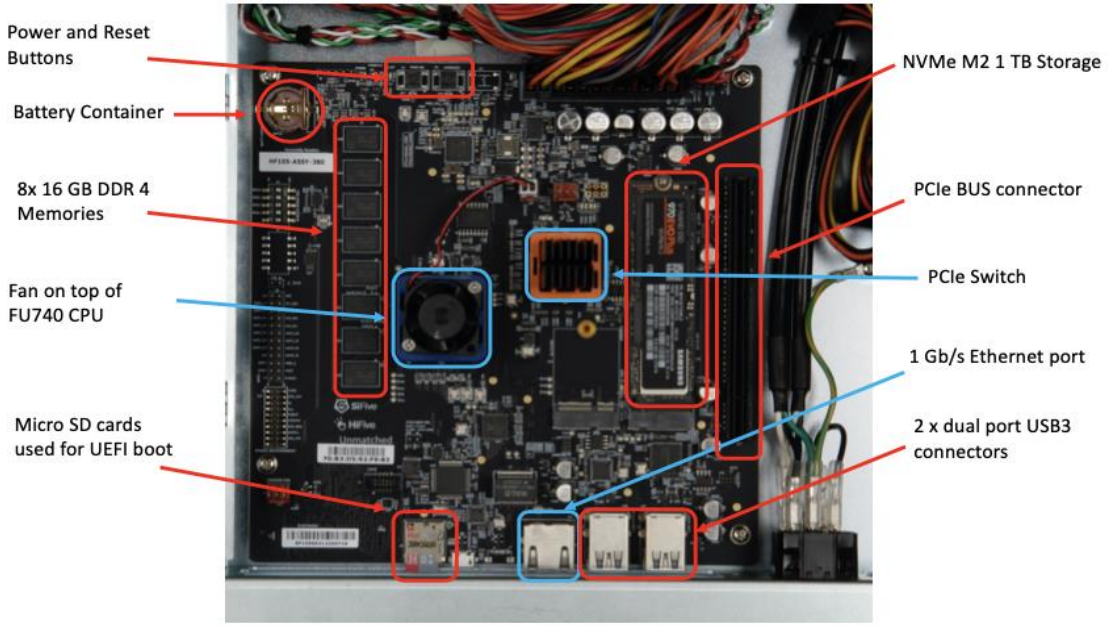
- UP to 3 x U280 FPGA
- Dual socket
- 128 core per socket @ 3GHz
- 32 DIMMs (8-channels 2DPC per CPU) Up to 8TB
- Max socket TDP: Up to 250W

TEXTAROSSA EU project aims at contributing to the strategic goals of the EuroHPC Strategic Research and Innovation Agenda and the ETP4HPC Strategic Research Agenda.

Key Features: Thermal Control, Energy Efficiency, High Performance, Easy Integration, Two-Phase Cooling Technology, Optimization of Multi-level runtime resource management.

E4 PROTOTYPE – MONTE CIMONE RISC-V CLUSTER

2022



https://www.e4company.com/en/2021/12/e4-announces-breakthrough-innovative-technologies-spanning-silicon-software-and-power-management-tools-integrated-in-the-risc-v-based-monte-cimone-cluster/

Preprint **"Monte Cimone: Paving the Road for the First Generation of RISC-V High-Performance Computers"** available online: http://arxiv.org/abs/2205.03725

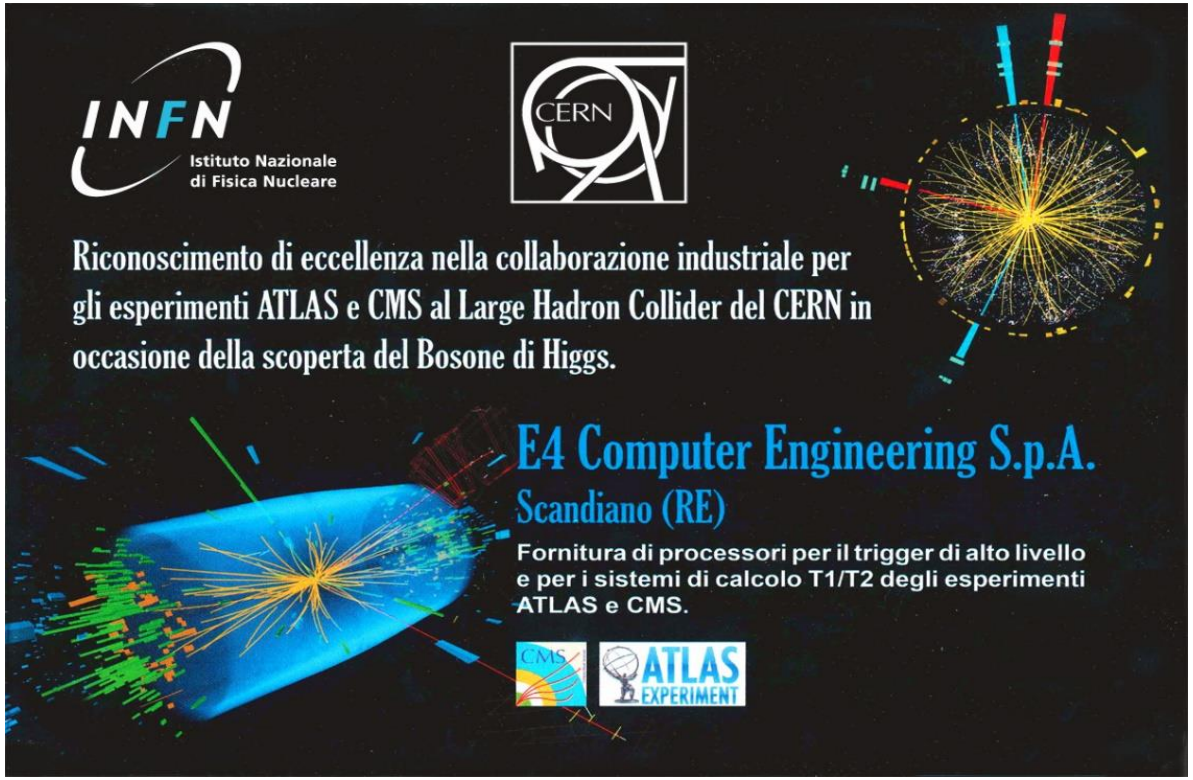
- **E4 is Strategic Member of the RISC-V Foundation**

E4 is at the forefront of the adoption of RISC-V

- The accelerator of EPI/SGA2
- Monte Cimone Cluster: Paving the Road for the 1st Gen. of RISC-V High-Performance Computers

- In-house R&D
- First real HPC cluster
- Early adopters as main target

RECOGNITIONS ON OUR COMPETENCES

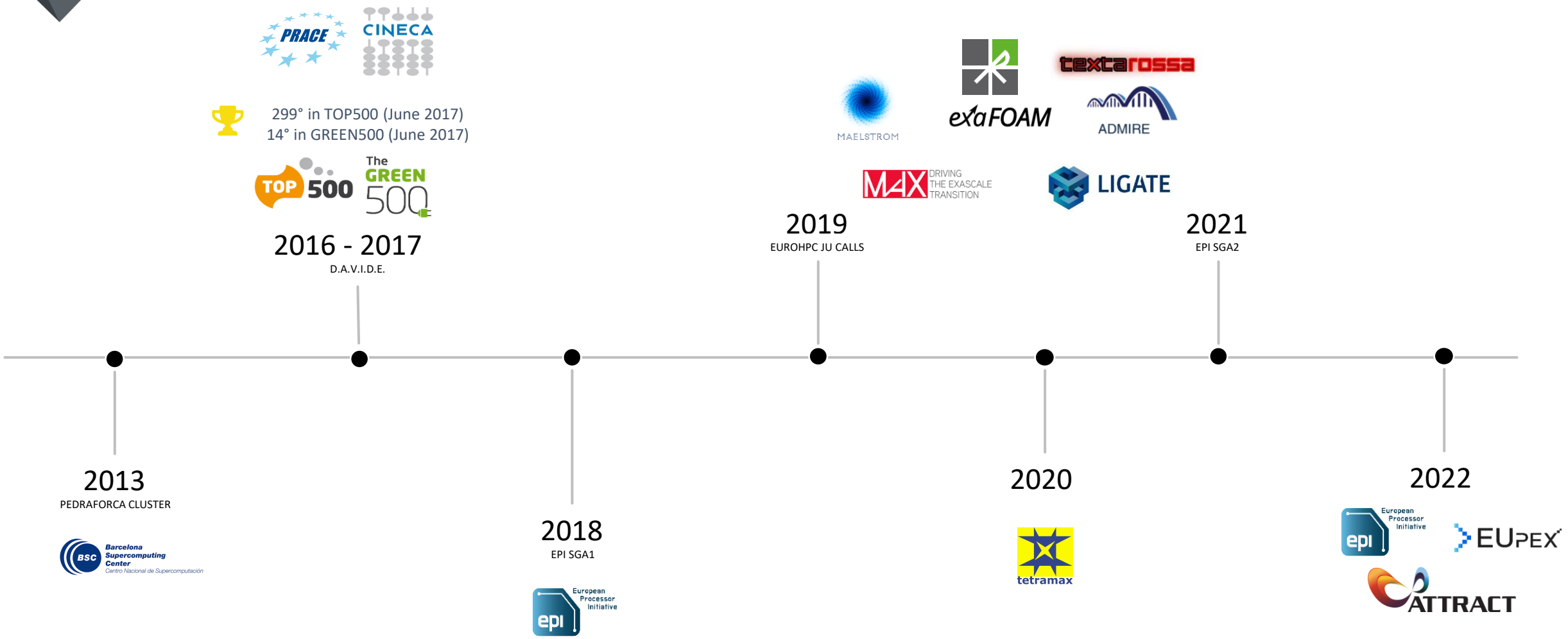


INFN & CERN AWARD (2012-2014)

Award of excellence in industrial collaboration for the **ATLAS** and **CMS** experiments at the Large Hadron Collider at **CERN** within the project of the discovery of the Higgs boson

EUROPEAN WIDE PRESENCE

WHERE WE CONTRIBUTE



E4
COMPUTER
ENGINEERING

GRAZIE
THANK YOU

E4 - ROLE IN EUROPEAN PROJECT

Design, build and validate the GPU blade
Build the GPP/GPU cluster
Co-design the second-generation EPI processors

Development and deployment of a Randomness farm: the Randomness Farm is based on a hardware embedding multiple generators in a scalable architecture, for infrastructural use. Hardware is complemented by a custom software development to guarantee a secure bit stream transmission, advanced real-time features and a set of services to maximize the adoption of the technology

Networking with potential users of codes
Visibility in the Material Science community
Know-how of the optimization techniques for the codes
Insight of the performance of the codes on a wide number of platforms

Contribution to the design and build of the PCIe EPAC Test Chip Daughter Board, of the RHEA Reference Platform and of the required additional components. Once this prototype reaches a sufficient level of stability and is ready for developers, E4 will also take care about the management and administration.

E4 - ROLE IN EUROPEAN PROJECT

textarossa

Developing a heterogeneous integrated development vehicles (idvs) featuring ARM and accelerator(s) (e.G. FPGA)
Defining the specification of the computing element in terms of processor, memory hierarchies and integrated IPS investigating both the MPSoC with embedded FPGA and the discrete PCIe-attached FPGA accelerator.

exaFOAM

Leading the evaluation of the performance of micro-benchmarks on homogeneous and heterogeneous architectures.
Leading the performance analysis and modelling of industrial use cases on relevant architectures.
To achieve this goals, e4 will provide hpc clusters of different architecture and with different types of accelerators.

ADMIRE

Development of Software Heritage (SH) Application
Testing, Deploying, and profiling of SH
Complete access for ADMIRE partners to the ARMIDA Cluster

LIGATE

Collecting requirements and specification from the different stakeholders, in particular industrial users and HPC centers for the evolution of HPC systems and EuroHPC infrastructures.
Defining the configuration and integration plan for the exascale CADD platform.
Expanding the applications (e.g. Gromacs, Ligen) to target clusters of GPUs.
Improving energy efficiency with more accurate energy measurements and cluster-level energy modelling.

MAELSTROM

Providing about 20 different HW configurations (including accelerated platforms) for development and testing of the machine learning tools.
Providing access to different storage architecture and technologies, the configuration of which will be the outcome of a co-design process.

E4 will contribute in requirements collection and co-designing of small-scale prototypes for the development and test of the applications. The two systems will be used also as small-scale evaluation platforms. E4 will integrate, together with Unibo the pulpcontroller into the REGALE prototype.

E4 MEMBERSHIPS

Strategic Members
https://riscv.org/

Member of CERN openlab
https://openlab.cern/

Member of the Steering Board
http://www.etp4hpc.eu

Member of the OEHI (Open Edge and HPC Initiative)
http://www.open-edge-hpc-initiative.org/

https://www.openfoam.com/

Member of HiPEAC
https://www.hipeac.net/

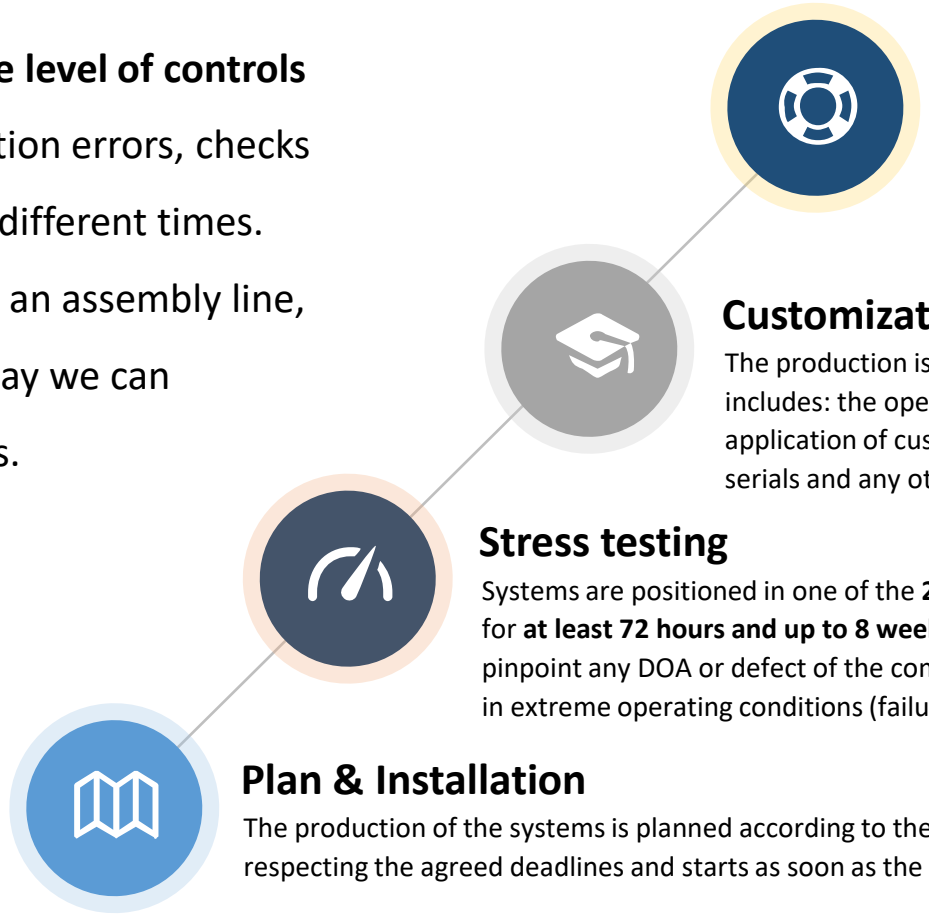
IN-HOUSE TECHNICAL APPROACHES

PERFESSIONALITY CREATES PERFECTION

E4 PROJECT APPROACH

The production cycle provides a **triple level of controls** to exclude possible human configuration errors, checks are carried out by different teams at different times.

The **entire cycle** is not managed with an assembly line, but is **structured by islands**: in this way we can guarantee the quality of our products.



Checking & Shipment

On a sample basis, the systems follow a simulation process of receipt at the customer, for which we **reproduce the entire cycle**: packaging, delivery to the customer, rack installation, ignition and testing.

Customization

The production is finalized with **a complete customization** of the product which includes: the operating system and applications chosen by the customer, the application of customized identification labels, collection and production of serials and any other customer request.

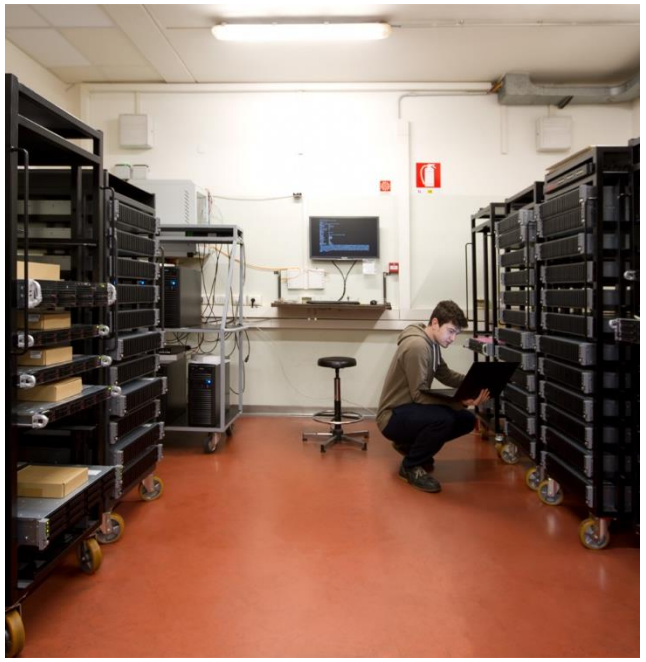
Stress testing

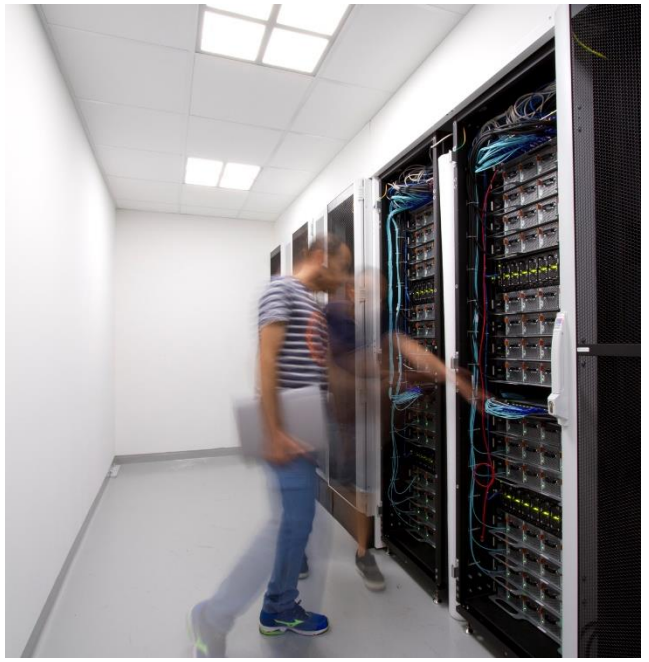
Systems are positioned in one of the **2 Burn-In test rooms** where they remain under stress test for **at least 72 hours and up to 8 weeks**. In these rooms the temperature is kept at 30 ° C to pinpoint any DOA or defect of the components and to **guarantee the stability of the systems** in extreme operating conditions (failure rate <1%).

Plan & Installation

The production of the systems is planned according to the customer's needs with the aim of respecting the agreed deadlines and starts as soon as the purchase order is received

E4 TECH FACTORY





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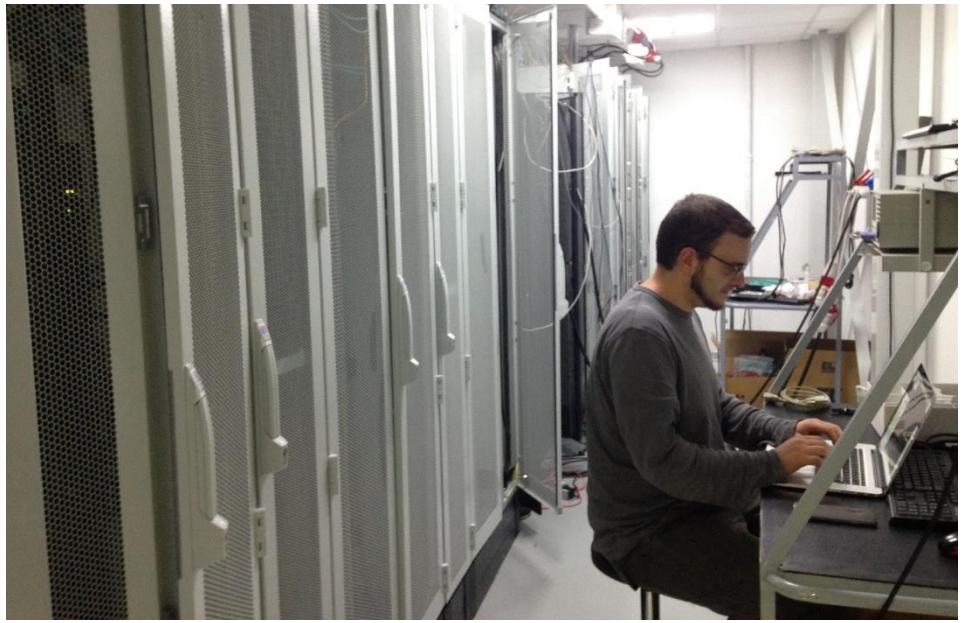

E4 PARTNERS


NVIDIA


AMPERE


Hewlett Packard
Enterprise


IBM


Micron


Mellanox
TECHNOLOGIES


SUPERMICRO


NetApp


ddn


run:
ai


arm


BeeGFS


XILINX


SOFTIRON


Atos


intel


AMD


DELL

E4 SKILLS AND COMPETENCES

Jira Service Desk

Confluence

RAPIDS

NVIDIA

DASK

intel

XILINX

AMD

OpenFOAM

Jenkins

slurm
workload manager

PBS

openstack

ANSIBLE

KOLLA

vmware

Bright Computing

VEEAM

docker

kubernetes

Red Hat

SPYDER

Visual Studio Code

APACHE Spark

RStudio

Microsoft

E4
COMPUTER
ENGINEERING

DELL

SUPERMICRO

CRAY
a Hewlett Packard Enterprise company

Hewlett Packard
Enterprise

AMPERE

Atos

IBM

GIGABYTE

Mellanox
TECHNOLOGIES

arm

sgi

ceph

PANASAS

BeeGFS

pandas

NetApp

ddn

Excelero

S3

POSIX

MINIO

PyCharm

jupyter

scikit learn

NumPy

SciPy

CONTACTS

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E4 Computer Engineering SpA

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